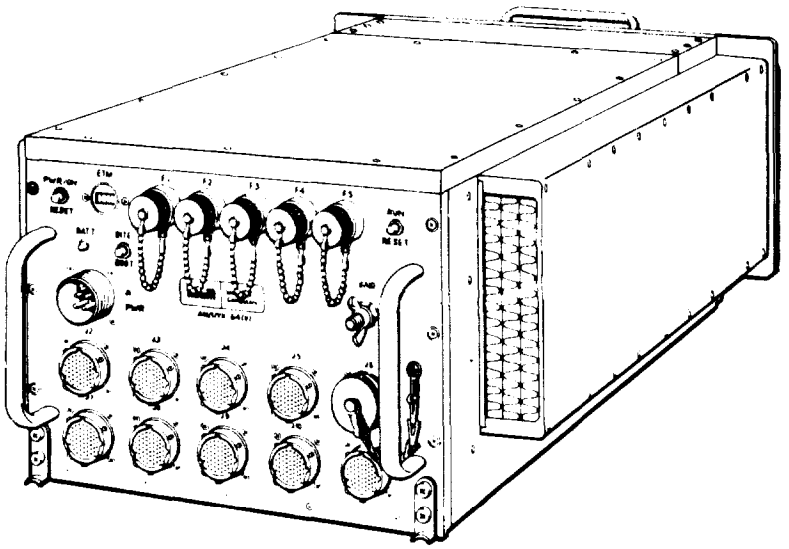
TM 11-7021-202-12

TECHNICAL MANUAL

OPERATOR'S AND ORGANIZATIONAL MAINTENANCE MANUAL



DATA PROCESSING SET

AN/UYK-64(V)1 (NSN 7035-01-155-0153)
AN/UYK-64(V)1x (NSN 7035-01-155-0154)
AN/UYK-64(V)2 (NSN 7035-01-166-7855)
AN/UYK-64(V)2x (NSN 7035-01-155-0155)
AN/UYK-64(V)3 (NSN 7035-01-155-0156)
AN/UYK-64(V)3x (NSN 7035-01-155-0157)
AN/UYK-64(V)4 (NSN 7035-01-155-0158)
AN/UYK-64(V)4x (NSN 7035-01-155-0159)

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HEADQUARTERS, DEPARTMENT OF THE ARMY
5 SEPTEMBER 1985

5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1 DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL

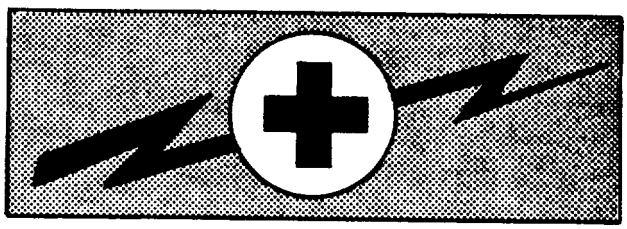
2 IF POSSIBLE, TURN OFF THE ELECTRICAL POWER

3 IF YOU CANNOT TURN OFF THE ELECTRICAL. POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A WOODEN POLE OR A ROPE OR SOME OTHER INSULATING MATERIAL

4 SEND FOR HELP AS SOON AS POSSIBLE

5 AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

WARNING



HIGH VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions

Never work on electronic equipment unless there is another person nearby who is familiar with the operation and hazards of the equipment and who is competent in administering first aid. When the technician is aided by operators, he must warn them about dangerous areas.

Whenever possible, the power supply to the equipment must be shut off before beginning work on the equipment. Take particular care to ground every capacitor likely to hold a dangerous potential. When working inside the equipment, after the power has been turned off, always ground every part before touching it.

Be careful not to contact high-voltage connections or 115 volt ac input connections when installing or operating this equipment.

Whenever the nature of the operation permits, keep one hand away from the equipment to reduce the hazard of current flowing through the body.

Warning: Do not be misled by the term “low voltage”. Potentials as low as 50 volts may cause death under adverse conditions.

For Artificial Respiration, refer to FM 21-11.

Technical Manual

NO. 11-7021-202-12

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 5 September 1985

Operator's and Organizational Maintenance Manual

DATA PROCESSING SET AN/UYK-64(V)

AN/JYK-64(V)1 NSN 7035-01-155-0153
AN/UYK-64(V)lx NSN 7035-01-155-0154
AN/UYK-64(V)2 NSN 7035-01-166-7855
AN/UYK-64(V)2x NSN 7035-01-155-0155
AN/UYK-64(V)3 NSN 7035-01-155-0156
AN/UYK-64(V)3X NSN 7035-01-155-0157
AN/UYK-64(V)4 NSN 7035-01-155-0158
AN/UYK-64(V)4X NSN 7035-01-155-0159

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in the back of this manual direct to: Commander, US Army Communications — Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, New Jersey 07703-5007. In either case, a reply will be furnished direct to you.

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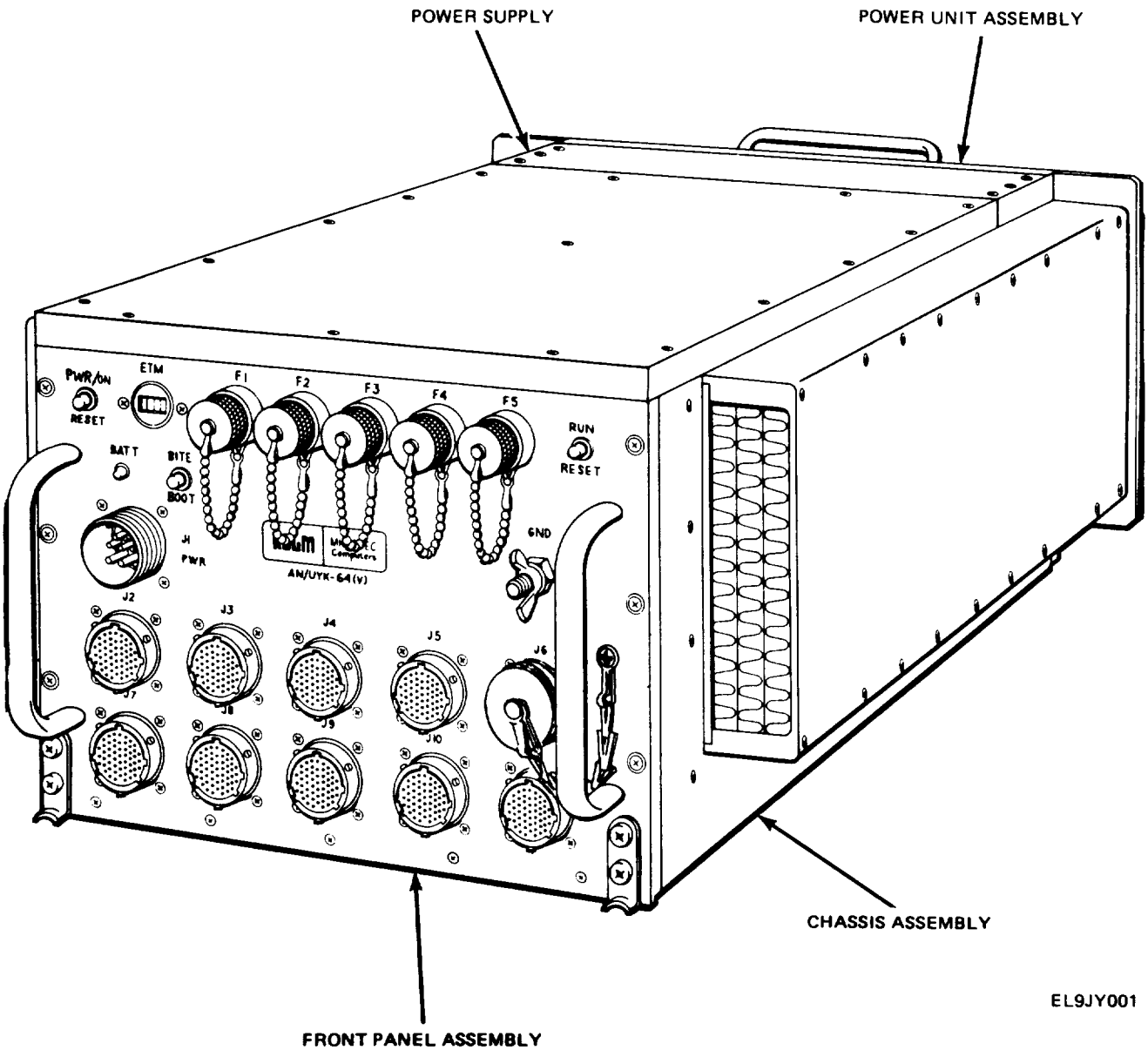


Figure 1. Data Processing Set AN/UYK-64 (V), Typical

CHAPTER 1

INTRODUCTION

Section L GENERAL INFORMATION

1-1. SCOPE

This manual contains detailed operating instructions and Operator/Organizational Maintenance information for Data Processing Set AN/UYK-64(V) (figure 1). Appendices to this manual provide a glossary, index, list of references, configuration data, and other items of information applicable to the operation and maintenance of Data Processing Set AN/UYK-64 (V). Except as otherwise noted, references to processor apply to all eight configurations (versions) of the Data Processing Set AN/UYK-64 (V); i. e., (V) 1, (V) 1X, (V) 2, (V) 2X, (V) 3, (V) 3X, (V) 4, and (V) 4X.

This chapter contains data relating to forms, records, and reports, and it provides general information that familiarizes the reader with the equipment. Equipment characteristics, capabilities, features, major component descriptions, and a discussion of equipment operating principles are included. Equipment interface information and instructions concerning safety, care, and handling of the equipment are also provided.

1-2. CONSOLIDATED INDEX OF ARMY PUBLICATIONS AND BLANK FORMS

Refer to the latest issue of DA PAM 310-1 to determine if there are new editions, changes, or additional publications pertaining to Data Processing Set AN/UYK-64 (V).

1-3. MAINTENANCE FORMS, RECORDS, AND REPORTS

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army form and procedures used for equipment maintenance are prescribed by DA Pam 738-750 as contained in Maintenance Management Update.

b. Reports of Packaging and Handling Deficiencies. Fill out and forward SF 364 (Report of Discrepancy (ROD)), as prescribed in AR 735-11 -2/DLAR 4140.55/NAVMATINST 4355.73A/AFR 400-54/MCO 4430.3F.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

1-4. ADMINISTRATIVE STORAGE

Equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the Preventive Maintenance Checks and Services (PMCS) charts in chapter 2 before being placed in administrative storage. When removing the equipment from

administrative storage, the PMCS should be performed to assure operational readiness. Disassembly and repacking of equipment for shipment or limited storage are covered in chapter 5.

1-5. DESTRUCTION OF ARMY ELECTRONICS MATERIEL

Destruction of Army electronics materiel to prevent enemy use shall be accomplished in accordance with TM 750-244-2.

1-6. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIRs)

If Data Processing Set AN/UYK-64 (V) needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about the processor. Let us know why you don't like the design. Put it on an SF 368, Quality Deficiency Report. Mail it to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, New Jersey 07703-5007. We will send you a reply.

1-7. OFFICIAL NOMENCLATURE, NAMES, AND DESIGNATORS

Table 1-1 provides a list of the processor major assemblies and subassemblies. The list identifies each item by its common name, official nomenclature, and equipment designator (if applicable).

Table 1-1. Nomenclature Cross-Reference List, AN/UYK-64 (V) Data Processing Set

Common Name	Official Nomenclature
Processor	Data Processing Set AN/UYK-64 (V) (Versions V1, V1X, V2, V2X, V3, V3X, V4, V4X)
Chassis/Mainframe	Processor Chassis Assembly (A25)
AC Power Supply	5617 AC Power Supply (A23)
DC Power Supply	5687 DC Power Supply (A23)
AC Power Unit	AC Power Unit Assembly
DC Power Unit	DC Power Unit Assembly
Front Panel	Front Panel Assembly (P/O Motherboard Assembly)

Section II. EQUIPMENT DESCRIPTION AND DATA

1-8. EQUIPMENT DESCRIPTION

The processor is one in a family of military computers supporting scientific and real-time applications requiring high speed processing and throughput. The processor provides proven reliability and high resistance to severe operating environments.

The processor is packaged in a single, conductively cooled air-transport rack (ATR) chassis/mainframe with wraparound heat exchanging. The chassis/mainframe provides an exit path for heat being generated by the power supply and printed-circuit boards (PCB). Cool air sucked in at the front of the processor is drawn through the air ducts on each side of the chassis absorbing heat as the air flows over the heat-conducting surfaces. The heated air is exhausted at the rear of the unit. Access for servicing the processor is facilitated by the removal of the power supply, front panel, and top and bottom cover plates.

Depending upon processor configuration (table 1-1), there may be either core or memory, configured with one of two types of Central Processing Unit (CPU) PROM printed-circuit boards (PCB), one of two types of Floating Point Unit (FPU) “C” PCB; and one of two types of motherboard processor may be powered by an ac or dc power supply. Additionally, a wide selection of input/output (1/0) interface PCB may be employed.

Eight input/output (I/0) slots are provided in the processors card cage for a maximum configuration of eight I/0 interfaces. The I/0 interfaces contain the interface logic and circuits that effect the two-way transfer of information and data between the processors CPU section and peripheral devices. It includes direct-memory access for high-speed devices.

A built-in test feature (BITE) provides a series of self-test diagnostics that are automatically performed at power-up as an aid in assuring processor readiness and the isolation of fault conditions.

A battery back-up feature for semiconductor memory configurations can be implemented to retain memory integrity in the event of power interruption.

Operator control of the CPU is provided through a system terminal when the CPU is in the virtual console (VC) mode. This mode permits boot/load operations, program loading, and diagnostic program loading. In addition, it provides the operator with the means of inserting break-points, examining and/or modifying the contents of a memory location or an internal software register, injecting standard program control functions, and the running of diagnostics.

1-9. EQUIPMENT CHARACTERISTICS, CAPABILITIES, AND FEATURES

Table 1-2 provides a list of the processor’s characteristics, capabilities, and features.

Table 1-2. Processor Characteristics, Capabilities, and Features

Item	Data
CPU	
Architecture:	Microprogrammed
Microinstruction Word Length:	64 bits
Microinstruction Capacity:	4096 Words
Instruction Length:	16 bits (single), 32 bits (double)
Hardware Accumulators:	4 Integer — 16 bits (optional)
Index Registers:	2 Integer — 16 bits
Instruction Types:	Fixed-Point Arithmetic Logical Operations Character Operations Floating Point
Addressing Modes:	Direct Immediate Indexed Program Counter Relative Accumulator Relative Multi-Level Indirect
Bus Structure:	Separate Memory In/Out I/O Prefetch Processor
SEMICONDUCTOR MEMORY	
Capacity	256k Words internal
Cycle Time:	500 nanoseconds
Interleaving:	2-way or 4-way
Module Capacity:	64k Words, 21 bits
Error Checking:	Single bit ERCC (5-bit code)

Table 1-2. Processor Characteristics, Capabilities, and Features — Continued

Item	Data
CORE MEMORY	
Capacity:	64k Words internal 960k Words external
Cycle Time:	1.0 microsecond internal 1. 1 microsecond external
Module Capacity:	32k Words, 17-bits
Error Checking:	Single bit, odd parity
INPUT/OUTPUT (1/0)	
I/O Types:	Programmed Data Channel
Interrupts:	16 Priority Interrupt Levels
Addressable Devices:	59
DIMENSIONS/WEIGHT	
Chassis:	7.62 in. x 13.30 in. x 24.19 in. (19.35 cm x 33.78 cm x 61.44 cm); 90 lb (40.90 kg).
ENVIRONMENT	
Units of the processor (system terminal excepted) are designed to the following environmental specifications, which meet or exceed those of MIL-E-5400 and MIL-E-16400.	
Inlet Air Temperature:	Standard: 0.0°C to + 50°C (+32°F to +105°F) Wide: -25°C to +60°C (+19°F to +140°F) Extreme: -55°c to +71°c (+41 °F to +159°F) (Core Memory only) (MIL-E-5400, Class 2, MIL-E-16400, Range 1)

Table 1-2. Processor Characteristics, Capabilities, and Features — Continued

Item	Data
Humidity:	95% relative
Vibration:	
With vibration isolators:	10g, 5-200 Hz (MIL-E-5400, Curve lVa)
Hardmounted:	2g, 5-2000 Hz (MIL-E-5400, Curve Ila)
Shock:	
With vibration isolators:	400 + lb impact (MlL-E-16400 and MIL-S-901C)
Hard mounted:	15g, 11 ms (MIL-E-400)
Altitude:	80,000 ft (MIL-E-5400, Class 2)
EMI Characteristics:	MIL-STD-461 A
Explosive Atmosphere:	Sand, dust, salt, fog, and fungus resistant in accordance with (MIL-E-5400 and MIL-E-16400.)
POWER	
Input Power:	100-130V ac, 47-63 Hz or 400 Hz, single-phase 220V ac (180-240), 47-63 Hz, single-phase 115V ac or 200V ac, 400 Hz, three-phase, MIL-STD-704C 208V ac (180-240), 47-63 Hz, three-phase 28V (24-32) (plus and minus)
Power Dissipation:	555 watts, Core memory version 575 watts, Semiconductor memory version 65 watts, Semiconductor memory during battery back-up (memory only)

1-10. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS

The processor (all versions) is comprised of the Chassis Assembly, power supply (ac or dc), Power Unit Assembly, and front panel (part of the Motherboard Assembly). Refer to table 1-1. The following subparagraphs provide component locations and descriptions:

a. Chassis Assembly. The chassis is comprised of the mainframe, card cage, two air ducts, and the top and bottom cover plates (fig. 1-1).

b. Power Supply. The 5617 AC Power Supply or a 5687 DC Power Supply is housed at the rear of the processor; behind and attached to the Power Unit Assembly. The power supplies are plug-in units. The AC Power Supply converts external primary 115V ac power into dc voltages required for processor operation. The DC Power Supply uses externally supplied 28V dc to create the dc voltages required for processor operation (fig. 1-1).

c. Power Unit Assembly. The Power Unit Assembly is mounted at the rear of the processor (fig. 1-2) and attaches to the chassis; the power supply is attached to the Power Unit Assembly. The ac version of the Power Unit Assembly is comprised of a cover, Power Unit (electronics module), and an ac blower fan. The dc version of the unit comprises the same components, except the electronics module is not used.

d. Front Panel Assembly. The front panel of a processor with semiconductor memory (fig. 1-1, 1-3) contains 11 connectors, a bank of five fuse assemblies, an Elapsed Time Meter (ETM), a PWR ON/RESET indicating pushbutton switch, program RUN/RESET indicating pushbutton switch, a BITE/BOOT indicating pushbutton switch, and a grounding lug. A BATT indicator shows whether or not the memory power (+5V) is up.

The front panel of a processor with core memory (fig. 1-1, 1-3) similar to the front panel of a processor with semiconductor memory with the following exceptions:

- No BATT indicator
- Ground stud moved from right side of the panel to upper left corner of the panel.
- J6 is converted from an 8-pin battery back-up connector to a 55-pin connector for interfacing an external core memory extension chassis.
- Panel is thicker and has a different shape than the panel on the semiconductor version (fig. 1-1).

Up to eight of the 11 connectors on the core memory processor front panel may be used to connect peripheral devices to their respective I/O interfaces PCB in slots Al through A8. The remaining three connectors are used for power input (ac or dc), connection to a system terminal, and connection to a remote memory. Three of the fuse assemblies on the panels are used when the processor is configured for ac power, and the remaining two are used when the input power is dc. The ETM display indicates accumulated processor running hours. Table 1-3 lists and describes the function of the processor's front panel connectors, indicators, controls, and fuses (fig. 1-3).

Table 1-3. Front Panel Connectors, Indicators, Controls, and Fuses

Item	Function
PWR ON/RESET Indicator	Indicating pushbutton switch. Indicates when prime power is applied; excluding battery back-up in a processor 1, 1X, 3, or 3X chassis. Pushbutton resets power after power has been interrupted.
ETM Display	Numerical display. Shows the accumulated time (Elapsed Time Meter) the processor has been running (power application); excluding battery back-up operating time in the processor 1, 1X, V3, or V3X chassis. Elapsed time is shown in hundreds of hours, plus first place decimal.
BATT Indicator	LED indicator. The indicator is lit to signify that the +5V memory bus is up; V1, 1X, 3, 3X only.
BITE/BOOT Indicator	Indicating pushbutton switch. Indicator is lit to signify that BITE self-testing was successful the last time it was executed. The pushbutton is also used to load (BOOT) the operating program from a dedicated external device.
RUN/RESET Indicator	Indicating pushbutton switch. Indicates when a program is running. Pushbutton is used to reset operating system and reinitialize the processor.
F1, Fuse Assembly	10 ampere, normal-blo fuse; Phase A leg of primary ac power wiring.
F2, Fuse Assembly	10 ampere, normal-blo fuse; Phase B leg of primary ac power wiring.
F3, Fuse Assembly	10 ampere, normal-blo fuse; Phase C leg of primary ac power wiring.
F4, Fuse Assembly	For core memory processors: 35 ampere, AGC 35 fuse. For semiconductor memory: 30 ampere, AGC 30 fuse. Part of the +28V power wiring.
F5, Fuse Assembly	For core memory processors: 35 ampere, AGC 35 fuse. For semiconductor memory: 30 ampere, AGC 30 fuse. Part of the +28V power wiring.
J1, 7-Pin PWR Connector	Power input connector used to connect externally supplied ac and dc voltages, plus system grounding.

Table 1-3. Front Panel Connectors, Indicators, Controls, and Fuses — Continued

Item	Function
J2, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A1 and the external system.
J3, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A2 and the external system.
J4, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A3 and the external system.
J5, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A4 and the external system.
J6, 8-Pin Battery Connector AN/UYK-64 (V) 1, 1X, 3, 3X	Connects a remote backup 28V battery supply for semiconductor memory configurations.
J6, 55-Pin Memory Connector AN/UYK-64 (V) 2, 2X, 4, 4X	Connects a remote memory for the expansion of memory in the core memory configurations.
J7, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A5 and the external system.
J8, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A6 and the external system.
J9, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A7 and the external system.
J10, 55-Pin I/O Connector	Provides I/O interface between I/O PCB A8 and the external system.
J11, 55-Pin System Terminal Connector	Provides system terminal command and control, between the processor and the system terminal.
GND Wing-Nut Stud	Provides a chassis ground connection capability.

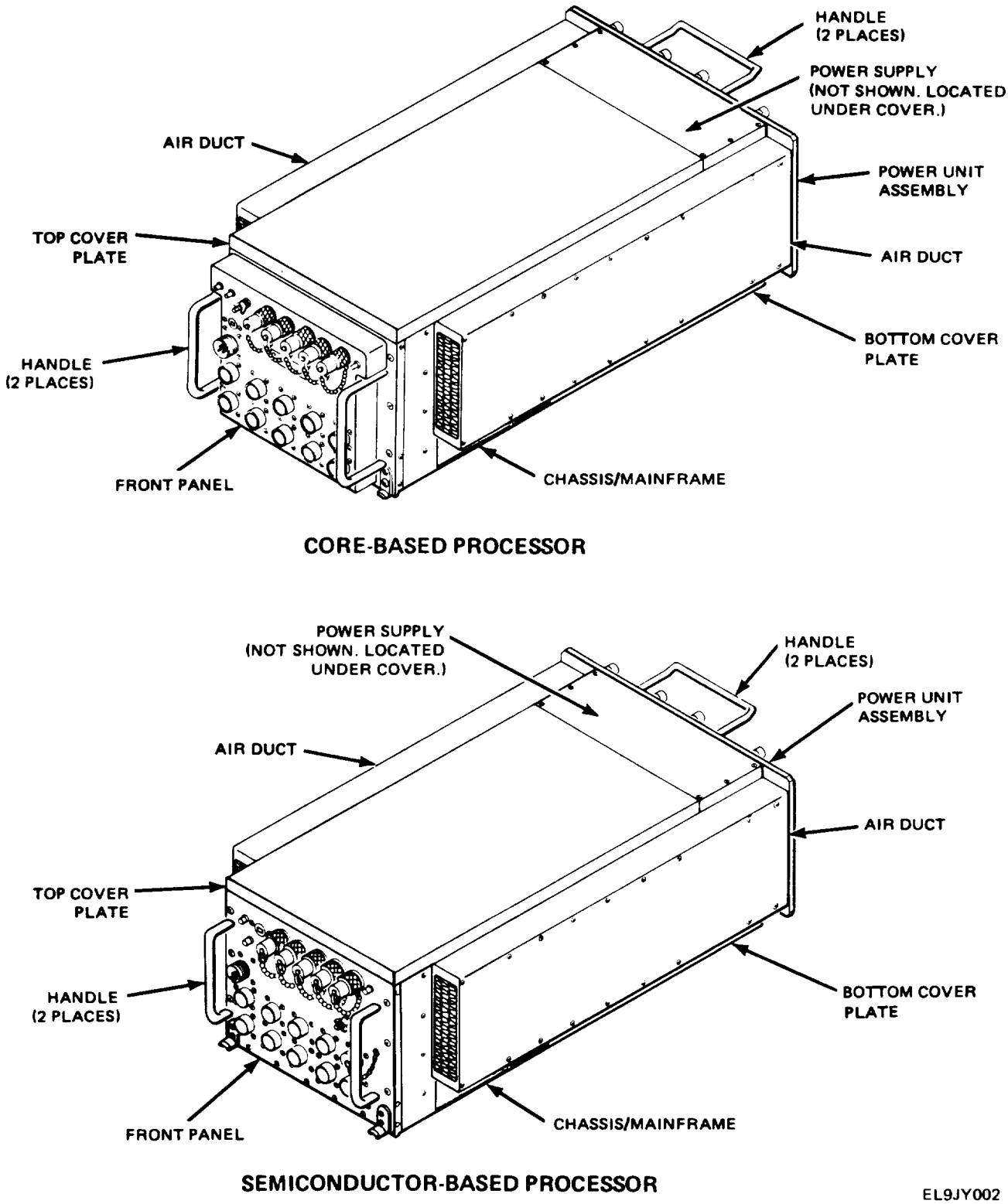
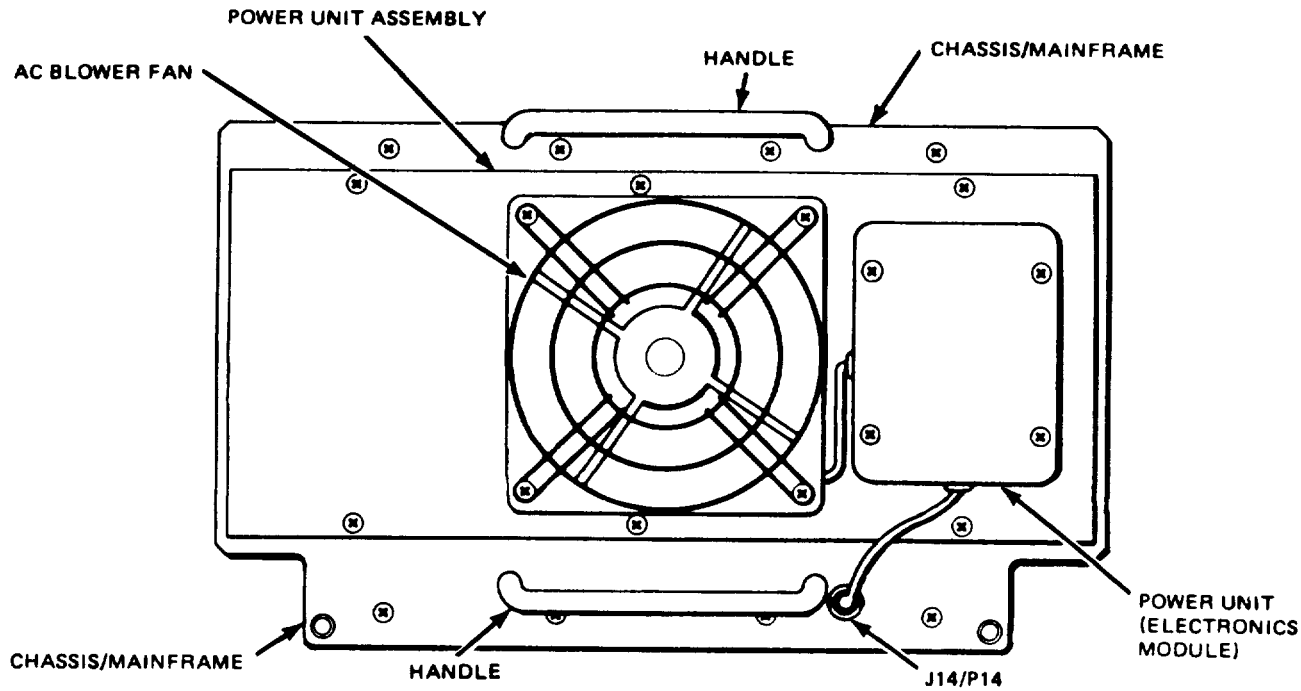
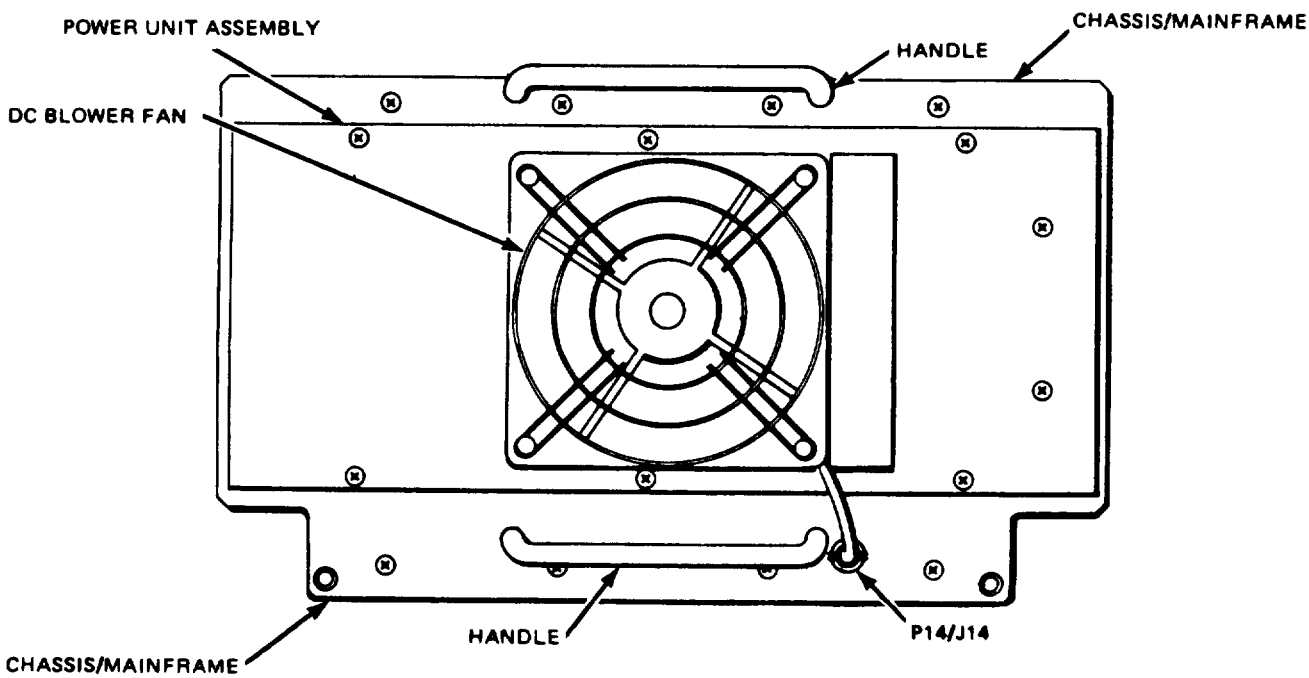


Figure 1-1. Processor, Semiconductor-and Core-Based, Component Locations



AC POWER UNIT ASSEMBLY (V1, V2, V3, V4)



DC POWER UNIT ASSEMBLY (V1X, V2X, V3X, V4X)

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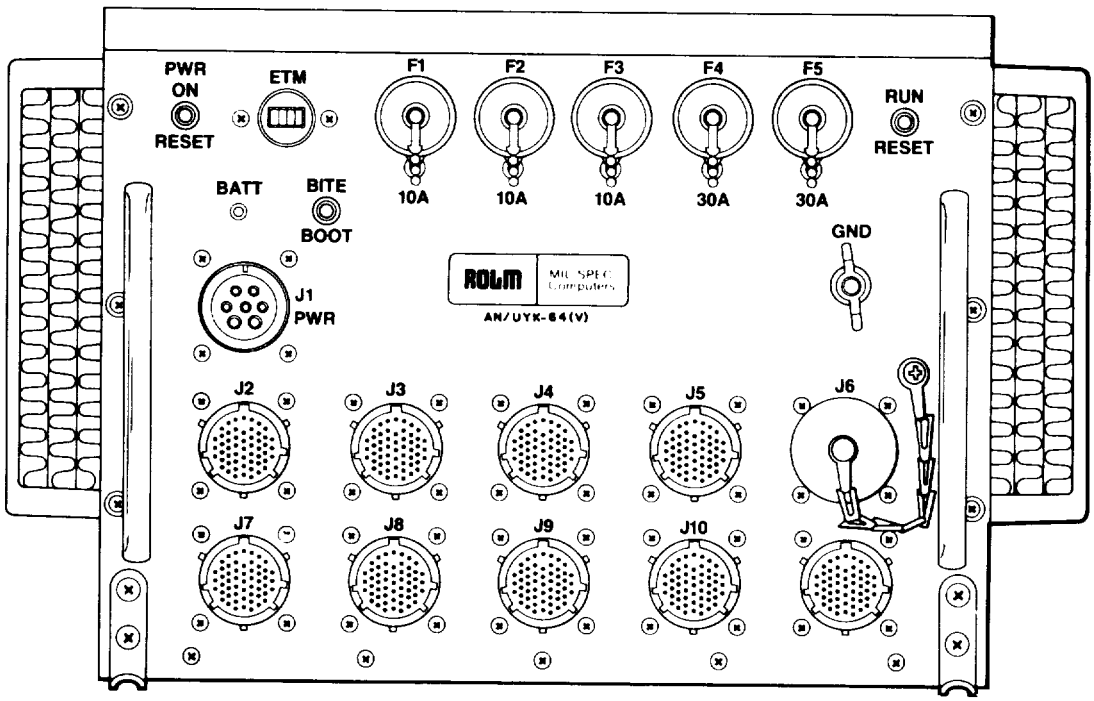
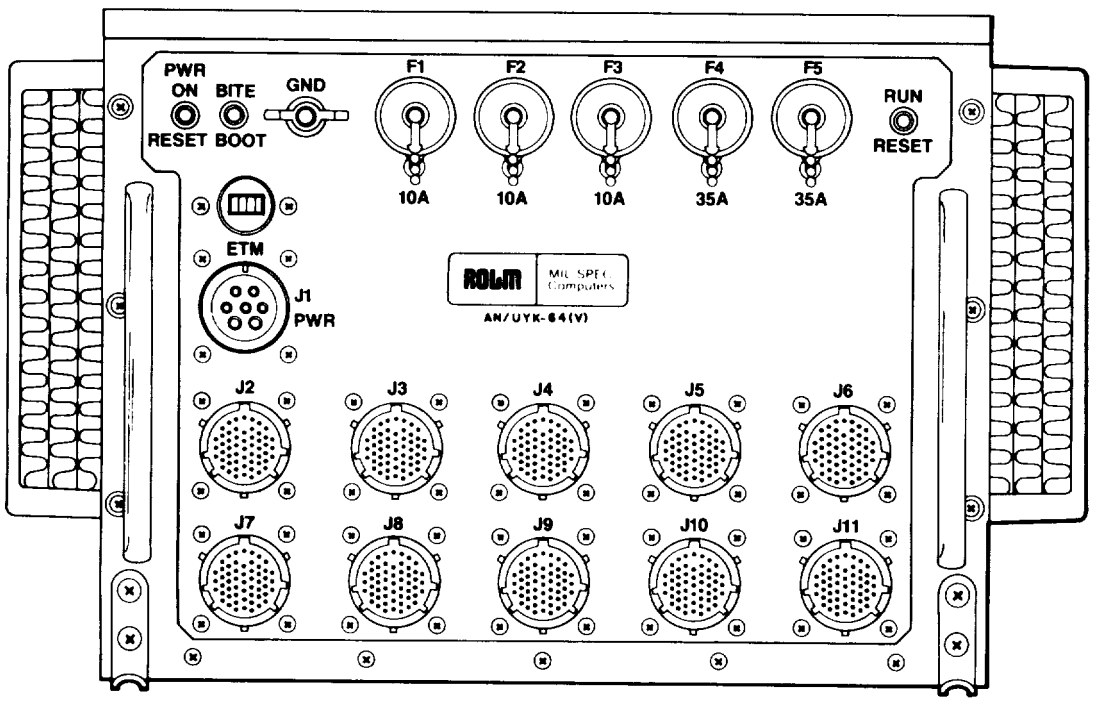
Figure 1-2. Processor Rear Views



SEMICONDUCTOR-BASED PROCESSOR (V1, V1X, V3, V3X)



CORE-BASED PROCESSOR (V2, V2X, V4, V4X)

Figure 1-3. Processor Front Panels

1-11. DIFFERENCES BETWEEN MODELS

Table 1-4 provides a matrix depicting the eight various configurations (versions) of the processor. Also, refer to paragraph 1-8.

1-12. EQUIPMENT CONFIGURATIONS

The following paragraphs discuss the various configurations (versions) of the processor and the system configurations in which the processor maybe deployed.

a. Processor Configuration. The primary differences between one version of the processor and any of the other seven versions are (table 1-4):

- Type of power system (ac or dc).
- Type of memory (core or semiconductor).
- Model of CPU PROM PCB (P/N 109836-01 or 109836-04).
- Model of FPU-C PCB (FPU-CE, P/N 109836-01 or FPU-C66, 11 0984-01).
- Model of Motherboard Assembly (P/N 109884-01 or 109885-02); includes Front Panel Assembly.
- The chassis configuration (P/N 110393-02 or 110815-02).
- Type of I/O PCB (appx G).

Of prime interest when considering processor configurations (versions) is the card cage. The paragraph to follow discusses the configuration of the processors' card cage.

b. Card Cage Configuration. The processor card cage consists of the core or semiconductor memory section, FPU section, CPU section, and the I/O section.

Although the card cage contains eight I/O board slots, the type of I/O boards used can vary considerably, according to the number and type of peripheral devices required in a specific system configuration.

c. Memory Configuration. The following subparagraphs discuss the processor memory configurations.

(1) Semiconductor memory. The memory size in a semiconductor-based processor is 256k Words. The word length is 21 bits, consisting of 16 data bits and a 5-bit error correction code. The 5-bit error correction code is generated by the A16 ERCC PCB during a memory-write cycle and is checked during a memory read-cycle. The memory cycle time is increased only if an error is corrected. The error code is transparent to the CPU. Semiconductor memory is volatile and cannot retain data integrity when there is a power interruption of up to 60 minutes.

Table 1-4. Data Processing Set AN/UYK-64 (V), Configuration Matrix

Assembly Number/ Model Description	Processor Configurations							
	VI	V1X	V2	V2X	V3	V3X	V4	V4X
PROCESSOR ASSEMBLY:								
112261-03	X	---	---	---	---	---	---	---
112261-07	---	X	---	---	---	---	---	---
112260-03	---	---	X	---	---	---	---	---
112260-07	---	---	---	X	---	---	---	---
110991-05	---	---	---	---	X	---	---	---
110991-11	---	---	---	---	---	X	---	---
110991-05	---	---	---	---	---	---	X	---
110991-11	---	---	---	---	---	---	---	X
MOTHERBOARD ASSEMBLY:								
109883-02	X	X	---	---	X	X	---	---
110800-02	---	---	X	X	---	---	X	X
CHASSIS ASSEMBLY:								
110393-02	X	X	---	---	X	X	---	---
110815-02	---	---	X	X	---	—	X	X
POWER SUPPLY:								
112676-01 (5687) DC Power	---	X	---	X	---	X	---	X
113081-01 (3884) DC EMI Filter	---	X	---	X	---	X	---	X
110684-01 (561 7) AC Power	X	---	X	---	X	---	X	---
112241-01 (3883) AC EMI Filter	X	---	X	---	X	---	X	---

Table 1-4. Data Processing Set AN/UYK-64 (V), Configuration Matrix — Continued

Assembly Number/ Model Description	Processor Configurations Assembly Number/							
	VI	V1x	V2	V2X	V3	V3X	V4	V4X
CORE MEMORY:								
109848-01 (1755) Controller	---	---	x	x	---	---	x	x
109550-01 (2019) Memory		---	x	x	---	---	x	x
SEMICONDUCTOR MEMORY:								
10984401 (1753) Controller	x	x	---	---	x	x	---	---
109840-01 (2030) Memory	x	x	---	---	x	x	---	---
109852-01 (1754) ERCC Controller	x	x	---	---	x	x	---	---
FLOATING POINT UNIT:								
109856-01 FPU-A	x	x	x	x	x	x	x	x
109860-01 FPU-B	x	x	x	x	x	x	x	x
110984-01 FPU-C66	x	x	x	x	---	---	---	---
100941-01 FPU-CE	---	---	---	---	---	x	x	x
CENTRAL PROCESSING UNIT:								
109824-01 DATA	x	x	x	x	x	x	x	x
109828-01 PFP	x	x	x	x	x	x	x	x
109836-04 PROM	x	x	x	x	---	---	---	---
109832-01 MAP	x	x	x	x	x	x	x	x
109836-01 PROM	---	---	---	---	x	x	x	x

(2) Core memory. The memory size in a core-based processor is 64k Words. The word length is 17 bits, consisting of 16 data bits and an odd parity bit. The A16 Internal Memory Control/Remote Memory Control (lMC/RMC) Controller PCB controls both internal and external memory. Core memory in non-volatile and retains data integrity for an indefinite duration, even with loss of prime power to the processor.

Core memory size can be increased in 32k Word increments; however, increase above the already contained 64k Words requires the addition of, and interfacing of, one or more remote memory chassis (through J6).

1-13. SAFETY PRECAUTIONS

The processor is a heavy piece of equipment. Three technicians are employed when moving the unit. Handles are provided on the processor as an aid when moving the processor. Use them (fig. 1-2, 1-3).

A periodic review of safety precautions in TB 385-4, Safety Precautions for Maintenance of Electrical/Electronic Equipment, is recommended. When the equipment is operated with covers removed, DO NOT TOUCH exposed connections or components. MAKE CERTAIN you are not grounded when making connections or adjusting components inside the test instrument.

Section III. PRINCIPLES OF OPERATION

1-14. INTRODUCTION

This section provides a brief explanation of processor operating principles.

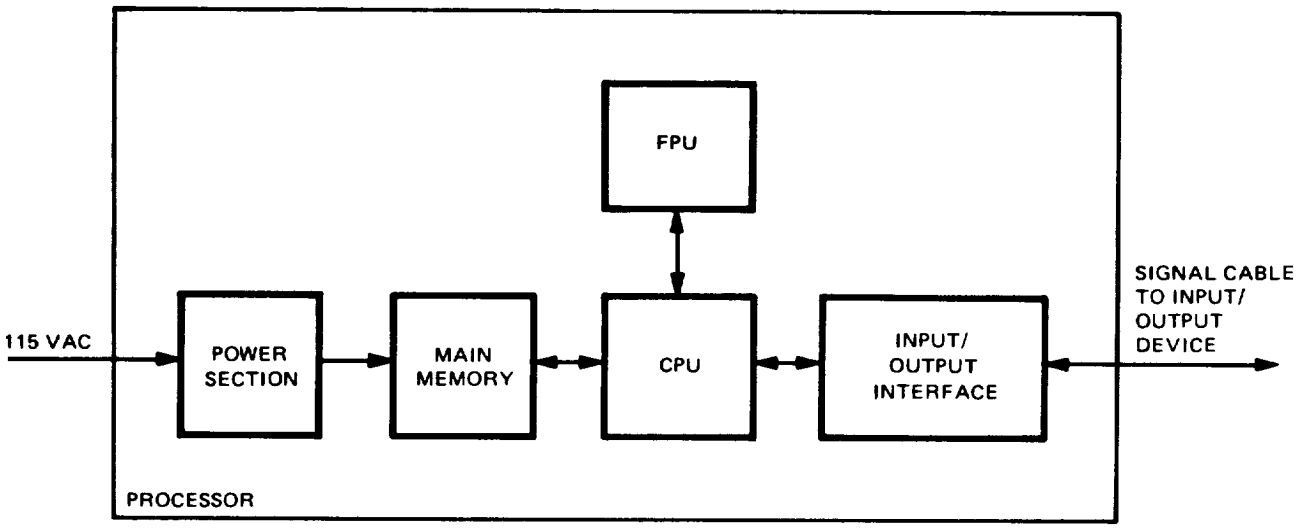
1-15. FUNCTIONAL OVERVIEW

The processor controls, processes, and interfaces data received from external devices. The processor can be divided into a power section, memory section, Floating Point Unit (FPU) section, Central Processing Unit (CPU) section, and an input/output (1/0) section. The paragraphs to follow provide information concerning the functioning of the sections mentioned. Additionally, the processing subsystems and bus functioning are discussed.

1-16. OPERATING PRINCIPLES

a. **Power Section.** The power section supplies the necessary dc power to run the processor. It operates from either 115V ac (47 to 440 Hz) using a 3883 AC EMI Filter and 5617 AC Power Supply, or 20 to 36V dc using a 3884 DC EMI Filter and 5687 DC Power Supply. Fuses F1, F2, and F3 provide overload protection when the processor is configured for ac power operation. Fuses F4 and F5 provide protection in the dc power configuration.

b. **Memory.** Memory is either semiconductor or core based, as specified in the processor configuration. The semiconductor memory size is 256k words and the core memory size 64k words.



NOTE: FOR DC OPERATION, AC EMI FILTER (3SS3) AND POWER SUPPLY (5617) IN PROCESSOR ARE REPLACED BY DC EMI FILTER (3884} AND DC POWER SUPPLY (5667).

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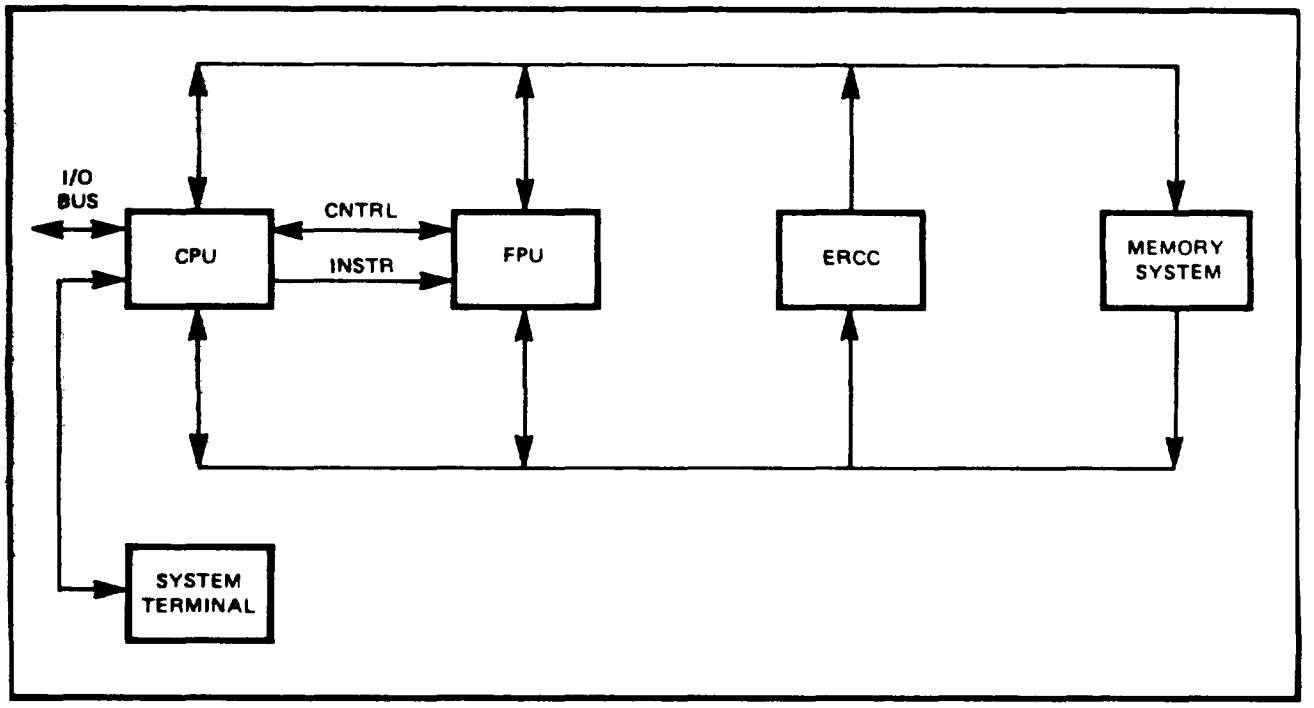
c. Floating Point Unit (FPU). The FPU section consists of three PCBs installed in the processor card cage. The FPU performs floating-point arithmetic on data supplied by the CPU and/or data in the internal floating-point accumulators. Data transfers to and from the FPU are controlled by the CPU, which also instructs the FPU as to the type of operation to be performed. The actual execution of the floating-point instruction is independent of the CPU. The FPU is monitored by the CPU to determine when the operation has been completed and the result is available. The FPU does not have direct access to memory.

d. Central Processing Unit (CPU). The CPU section consists of four PCBs. It decodes and initiates execution of all instructions and performs all fixed-point arithmetic and memory-reference operations. Its principal functional components include the Arithmetic Logic Unit (ALU) and its input and output bus, the Prefetch Processor (PFP) and its bus, the asynchronous communications interface for the system terminal, and the memory bus interfaces.

e. Input/Output Section. The input/output (I/O) section is made up of processor slots—A1 through A8. Interface modules are installed in these slots to allow the processor to interface with equipment external to the processor.

f. Major Subsystems and System Buses. The diagram to follow shows a simplified representation of the functional sections (subsystems) within the processor and the principal buses over which data is exchanged between the sections. There are two principal internal buses: Memory In (MEMIN) and Memory Out (MEMOUT), and one principal external bus, the I/O Bus.



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The two internal buses handle ail data exchanges between the subystems. The MEMIN bus carries address and write data to the memory system and also carries information from the CPU to the FPU. The bus is unidirectional and 21 bits wide, which permits physical addressing of 2048k words in core memory systems and the transfer of 16-bit data words in both semiconductor and core memory based systems. The illustration on the previous page depicts a semiconductor-memory based system, which accommodates a 21-bit word (15 data bits, plus a 5-bit error code). In core-memory systems, a 17-bit word is stored (16 data bits plus an odd parity bit). The MEMOUT bus is essentially a 16-bit unidirectional bus and carries data and instructions read from memory to the CPU, programmed I/O information and data from the CPU to the I/O interfaces, and floating-point information from the FPU to the CPU. The I/O Bus interfaces with both of the memory buses for the purposes of direct memory access and I/O transfers under CPU supervision.

The I/O bus carries all command and data transactions between the processor and peripheral device interfaces. The transactions are of two types: Programmed I/O and Direct Memory Access (DMA). Programmed I/O operations are initiated by the CPU to execute a software instruction. The operation may involve a transfer of data to or from an I/O interface, the transmission of a control command from the CPU to the device including functional parameters, or the retrieval of the device status. DMA operation is initiated by the CPU, but involves the transfer of data between the I/O interface and memory without CPU intervention. For both programmed I/O and DMA transfers, 16 bidirectional data lines within the I/O bus are used. The remaining lines within the bus are used for control and device selection functions. A communications line connects the system terminal to the Universal Asynchronous Receiver/Transmitter (UART) in the CPU. This line is dedicated to the system terminal.

The CPU coordinates the operations of all the other subsystems by status and control lines. The CPU executes all memory data references and instruction fetches by means of its mapping logic, which translates a 15-bit or 16-bit logical address into a 20-bit physical address, places the address on the MEM IN bus, and requests the appropriate memory cycle.

The MAP logic checks for violation of one of several types of protection. If a violation is detected, the CPU is notified and a protection trap ensues. If the memory cycle involves a write-to-memory, the CPU places the data on MEMIN within specified timing constraints. If a memory-read operation is involved, as in the case of an instruction fetch, the memory places the data on the MEMOUT bus and the CPU takes the data from the bus at the specified time.

After the CPU has received the data from an instruction fetch, the instruction is decoded and the appropriate action is taken. If the instruction required memory references, the CPU will execute them as described. Accumulator-to-accumulator operations, including fixed-point arithmetic, are executed entirely within the CPU.

g. Bus Utilization. Floating-point arithmetic instructions involve both the CPU and FPU for their execution. The CPU may determine the status of the FPU by retrieving the FPU status word on the MEMOUT bus, The status may be changed by the CPU and sent to the FPU on the MEMIN bus. While the memory buses are being used in this fashion, memory reference cycles are inhibited. If the CPU needs to provide the operands, they are transferred to the FPU on the MEMIN bus. If memory is to provide one or both operands, they are obtained from memory on the MEMOUT bus and transferred to the FPU, in which case the CPU and not the FPU provides the memory address. If the result is required by the CPU, it is transferred from the FPU on the MEMOUT bus. If the result is to be stored in memory, the memory address (MEMIN) is supplied by the CPU and the result is supplied by the FPU (MEMIN). The actual instruction is transferred directly from the CPU to the FPU on dedicated instruction lines, as are control signals. Note that the FPU does not have direct access to memory. Memory addresses required during a floating-point arithmetic operation are provided by the CPU and not the FPU.

In terms of Output operations (I/O), the 16 bidirectional data lines of the I/O bus can be considered as an extension of MEMOUT in the one direction. During Input operations, MEMIN can likewise be considered as an extension of the 16 data lines in the opposite direction, taking into account proper interfacing in both directions.

In programmed I/O operation (Output), the CPU sends commands, control functions, and data to the device through the I/O bus and I/O interface. In the case of data transfers, the CPU first reads the data from memory into an accumulator, then transfers the data from the accumulator to the I/O interface. In Input operations, the CPU receives data and status information from the device through the I/O interface and I/O bus in response to a previously issued command. Data or status information is read into an accumulator, and in the case of data transferred to memory, from the particular accumulator. Status information is processed by the CPU to determine what course of action to take, according to the device service routine.

Before an actual DMA operation can take place, the subject device is given the starting address of a memory data buffer (to or from which data is to be transferred), the number of words or bytes to be transferred, and finally the operational command. This takes place in identical fashion to programmed I/O, according to the particular service routine. The information is obtained from memory by the CPU (MEMOUT) and sent from the CPU to the device through the I/O bus and I/O interface. Once the DMA operation commences, memory addresses are supplied by the device and appear on MEMIN. The direction of data flow depends on the operation being performed. For example: when a write command is issued to a magnetic tape unit (MTU), data is read from memory as though there were a direct path from memory (MEMOUT) to the MTU. When a read command is issued, data is read from the tape and written into memory (MEMIN), again as though there were a direct data path. Note that the I/O device supplies the memory address by using increments of the start address.

CHAPTER 2

OPERATING INSTRUCTIONS

Section L GENERAL INFORMATION

2-1. GENERAL

This chapter provides instructions for operating Data Processing Set AN/UYK-64 (V). Additionally, the chapter contains required preventive maintenance information.

2-2. ARRANGEMENT OF CHAPTER

The content of this chapter is presented in sections as follows:

- Section I. General Information
- Section II. Operator Preventive Maintenance Checks and Services (PMCS)
- Section III. Operation Under Usual Conditions
- Section IV. Operation Under Unusual Conditions

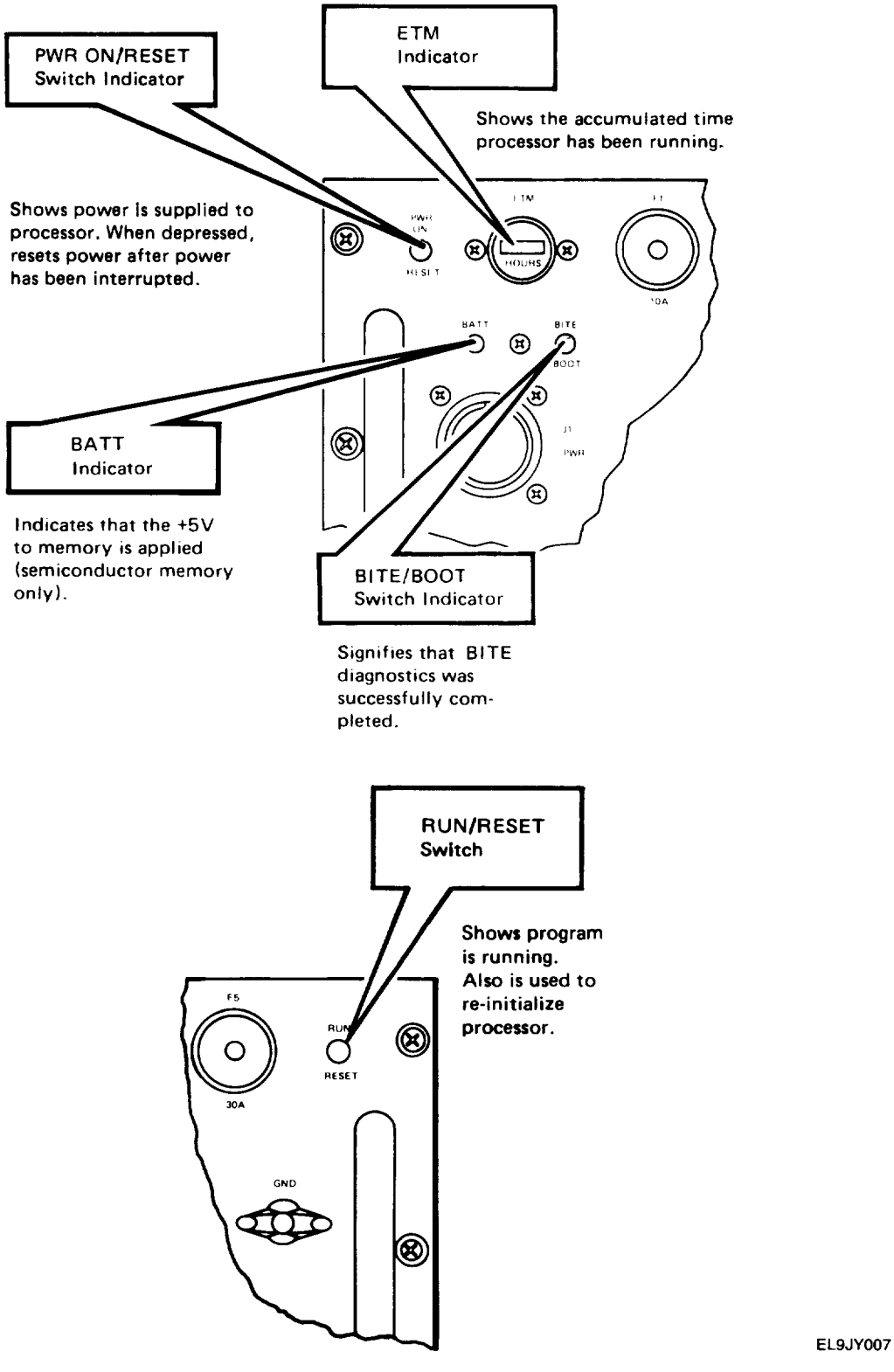
2-3. DESCRIPTION OF OPERATOR'S CONTROLS AND INDICATORS

Operators and maintenance technicians must be familiar with the purpose, function, and general physical characteristics of the processor before attempting to operate or perform maintenance on the unit. Chapter 1 must be studied in its entirety prior to proceeding further.

WARNING

Do not operate equipment without a suitable ground connection. Electrical defects in the unit, test equipment, or load equipment can cause DEATH by electrocution when contact is made with an ungrounded system.

The following narrated illustrations provide a description, the location, and the use of the operator's controls and indicators on the processor (table 1-3).



Section II. OPERATOR PREVENTIVE MAINTENANCE CHECKS AND SERVICES (PMCS)

2-4. INTRODUCTION

The maintenance duties of the Operator include the performance of Preventive Maintenance Checks and Services (PMCS). PMCS are the systematic care, servicing, and inspection of equipment to prevent trouble and reduce downtime by detecting operational problems. PMCS are required to maintain Army electronic equipment in a combat serviceable and mission-ready condition. PMCS are performed:

- **Before Operation.** Always keep in mind the CAUTIONS and WARNINGS noted throughout this manual. Perform the before (B) PMCS.
- **During Operation.** Always keep in mind the CAUTIONS and WARNINGS noted throughout this manual. Perform the during (D) PMCS.
- **After Operation.** Be sure to perform the after (A) PMCS.
- **If Processor Fails to Operate.** Troubleshoot with proper equipment. Report any deficiencies using the proper formS (DA Pam 738-750).

a. PMCS Table. The following subparagraphs define the purpose of the PMCS table, service intervals, and procedure columns. Also provided are Operator instructions for reporting equipment operating deficiencies.

(1) Purpose of PMCS table. The PMCS table 2-1 lists the inspections and care of the equipment which are performed by the Operator to ensure that the equipment remains in the proper operational readiness.

(2) Service Intervals. The INTERVAL column of the PMCS table 2-1 informs the Operator as to how often checks and services are to be performed. Following is an explanation of the internal codes:

NOTE

ALL PMCS must be done as regularly scheduled and also under the following conditions:

- When the processor is first installed.
- Processor is being operated for the first time.
- When the processor is reinstalled after being removed for any reason.
- Before the processor is used on a mission.

BEFORE OPERATION — Do the (B) PMCS before operating the processor.

DURING OPERATION — Do the (D) PMCS during the operation of the processor.

AFTER OPERATION — Do the (A) PMCS after operating the processor.

WEEKLY — Do the (W) PMCS weekly.

(3) Procedure column. The PROCEDURE column of PMCS table 2-1 shows the Operator how checks and services are to be performed. Instructions are to be carefully followed.

(4) Equipment Not Ready/Available If: Procedures. The EQUIPMENT NOT READY/AVAILABLE IF column of PMCS table 2-1 informs the Operator when the equipment cannot be used and why it cannot perform the assigned mission requirements, If the equipment fails to operate as required, refer to chapter 3 for maintenance instructions. Report any malfunctions on DA Form 2404 (DA PAM 738-750).

NOTE

The terms “ready/available” and “mission capable” refer to the same status; equipment is on hand and is able to perform its combat missions (DA PAM 738-750).

b. Special Instructions. if the processor must be in use most of the time, check and service those items that can be checked and serviced without stopping its operation. Make complete checks and services only when the processor is finally shut down.

c. Deficiency Reporting and Correcting. Should the equipment fail to operate properly, the Operator reports the problem to Organizational Maintenance for corrective action. Ail such equipment failures are recorded on DA Form 2404 (DA PAM 738-750).

d. Equipment Removal. There is no requirement for the Operator to remove the processor in order to perform the PMCS.

e. Tools, Materials, and Equipment Required for Maintenance. No tools or equipment are required for Operator Maintenance. The following cleaning materials are required (appx D):

- Lint-free cloth (item 3, appx E)
- Soft bristle brush (item 2, appx E)
- isopropyl alcohol (item 1, appx E)
- Detergent (item 4, appx E)

f. Routine Services. Routine services are a collection of checks and observations performed by the Operator. Routine services are not listed in the PMCS table 2-1 in order to separate the nonoperational from the operational services. Refer to chapter 3 for additional information. The Operator will perform the following routine services as necessary:

- Clean
- Dust
- Check for cut or frayed cables.
- Check for rusting and corrosion.
- Check controls for smooth operation.
- Check for unusual odors (e.g., overheating of processor, smoke, etc.).
- Check for loose nuts, bolts, and connectors.
- Check for completeness of equipment.
- Check for noisy blower fan.

EQUIPMENT INSPECTION AND MAINTENANCE WORKSHEET

For use of this form, see TM 38-750: the proponent agency is the Office of the Deputy Chief of Staff for Logistics.

1. ORGANIZATION	2. NOMENCLATURE AND MODEL

3. REGISTRATION/SERIAL/FSN	4a. MILES	b. HOURS	c. ROUNDS FIRED	d. HOT STARTS	5. DATE	6. TYPE INSPECTION

7. APPLICABLE REFERENCE

TM NUMBER	TM DATE	TM NUMBER	TM DATE

INSTRUCTIONS: Perform each check listed in the TM applicable to the inspection performed. Following the sequence listed in pertinent TM, complete form as follows:

COLUMN a - Enter TM item number.

COLUMN b - Enter the applicable condition status symbol.

COLUMN c - Enter deficiencies and shortcomings.

COLUMN d - Show corrective action for deficiency or shortcoming listed in Column c.

COLUMN e - Individual ascertaining completed corrective action initial in this column.

ALL INSPECTIONS AND EQUIPMENT CONDITIONS RECORDED ON THIS FORM HAVE BEEN DETERMINED IN ACCORDANCE WITH DIAGNOSTIC PROCEDURES AND STANDARDS IN THE TM CITED HEREON.

8a. SIGNATURE (Person(s) performing inspection)	8b. TIME	9a. SIGNATURE (Maintenance Supervisor)	9b. TIME	10. MAN HOURS REQUIRED

TM ITEM NO	STATUS	DEFICIENCIES AND SHORTCOMINGS	CORRECTIVE ACTION	INITIAL WHEN CORRECTED

USE PMCS ITEM NO

Table 2-1. Operator Preventive Maintenance Checks and Services

B = Before Operation **D =** During Operation **A =** After Operation **W =** Weekly

Item No.	Interval				Item To Be Inspected/ Procedure	Equipment Is Not Ready/Available If:
	B	D	A	W		
1	•	•			**PWR ON/RESET** indicator: Check to see that light turns on when power is applied or system is reset.	Power not supplied to processor.
2	•	•			**FAN:** Listen for proper operation.	Fan does not run.
3	•	•			**BATT** indicator: Check to see that light is lit whenever power is applied to processor (semiconductor memory units only).	**BATT** indicator won't light.
4	•		•		**BITE/BOOT indicator:** Check to see that light is lit after BITE is completed.	**BITE** indicator won't light.
5	•	•			**RUN/RESET** indicator: Check to see that light is lit when program is running.	
6		•		•	**ETM** indicator: Check to see that ETM indicator is functioning.	

Section III. OPERATION UNDER USUAL CONDITIONS

2-5. INTRODUCTION

This section provides instructions for operating the processor under usual conditions. Should equipment operating problems arise when attempting to use the processor, report the malfunction on DA Form 2404 (DA PAM 738-750).

WARNING

Do not operate equipment without a suitable ground connection. Electrical defects in the unit, test equipment, or load equipment can cause **DEATH** by electrocution when contact is made with an ungrounded system.

HIGH VOLTAGE is used in this equipment. **DEATH ON CONTACT** may result if safety precautions are not observed.

2-6. INITIAL ADJUSTMENTS, DAILY CHECKS, AND SELF-TEST

Initial adjustments on the processor are beyond the scope of this manual. The Operator performs the PMCS described in section II of this chapter on a newly installed processor before operating. The BITE self-test runs automatically each time power is applied to the processor as an initial operational checkout.

2-7. OPERATING PROCEDURES

a. Preliminary Procedures.

NOTE

The processor does not have a main power circuit breaker. Power is applied to the processor as soon as the power cable is connected to a power source. The PWR ON/RESET indicator pushbutton lights to indicate that power is supplied (para 2-3). At power up, the CPU automatically performs the BITE sequence of self-test diagnostics. The BITE/BOOT indicator lights when the BITE tests have been successfully completed. It takes about 15 seconds for BITE to run.

1. Connect processor to prime power source. Verify that the PWR ON/RESET indicator is lit. If the processor has semiconductor memory, verify that the BATT indicator is also lit.

2. Ensure that PMCS have been accomplished before operating the equipment (para 2-4).

b. Power-Up Procedure.

(1) Depress PWR ON/RESET pushbutton switch to reset the unit (para 2-3).

NOTE

If for any reason the BITE indicator does not light, refer the problem to Organizational Maintenance for corrective action.

(2) Verify that after a short delay of about 15 seconds, the BITE/BOOT indicator lights to indicate that the processor has successfully completed the self-test diagnostics (para 2-3).

c. Operating Procedure.

(1) Connect power cable to power source and to the processor. Verify that the PWR ON/RESET indicator is lit. If processor has semiconductor memory, verify that the BAIT indicator is also lit.

(2) Depress PWR ON/RESET pushbutton switch.

(3) BITE/BOOT indicator should go out when PWR ON/RESET switch is depressed, and light again when the self-test is completed (after about 15 seconds).

NOTE

If the BITE indicator does not light, refer the problem to Organizational Maintenance for corrective action.

(4) Verify that the ETM indicator is operating properly by observing the movement of the flag between the first and second digits.

(5) Bring the processor on line with the system in accordance with instructions contained in the applicable system manual.

d. Turn Off Procedures. Refer to applicable system manual or disconnect processor from power source, if necessary.

e. Emergency Stopping Procedure. In case of emergency, immediately disconnect the processor from the power source.

Section IV. OPERATION UNDER UNUSUAL CONDITIONS

2-8. OPERATION IN UNUSUAL WEATHER

It may be necessary to operate the processor under abnormal conditions where extreme cold, heat, humidity, moisture, or sand and dust conditions prevail. Instructions for minimizing the effects of these unusual operating conditions are given in the following subparagraphs.

a. Arctic Climates. Subzero temperatures and climatic conditions effect the proper operation of the equipment. Handle the equipment carefully. Parts, especially plastics and wiring insulation, become brittle at subzero temperatures. When equipment is exposed to cold air, moisture will condense on it. Dry the equipment thoroughly. Equipment should be operated in a heated environment (table 1-2).

b. Tropical Climates. In tropical climates, the high relative humidity causes condensation of moisture on the unit whenever equipment temperature becomes lower than that of the surrounding air (table 1-2). Adequate ventilation will minimize this condition. Check frequently for fungus or moisture on the unit. To remove fungus or moisture, use a lint-free cloth and alcohol.

c. Desert Climates. The main problem arising in desert operation is sand, dust, or dirt getting into the equipment. Keep the equipment as free of foreign material as possible.

2-9. EMERGENCY PROCEDURES

In the event of a power outage, data currently stored in the processor's semiconductor memory may be lost. The RAM chips used in the semiconductor memory do not hold information in the event of a power failure; however, a battery backup unit can be connected to the processor. Battery backup power is connected at J6 on a semiconductor-based processor and can maintain the memory for approximately 60 minutes (table 1-3).

The magnetic nature of the core memory module allows it to hold current instructions and operating data, unchanged, in the event of a power outage. No backup battery is required for processors with core memory.

If an emergency condition occurs, shut down main power source to the equipment. Refer to the applicable system manual for additional emergency shut-down procedures.

CHAPTER 3

OPERATOR'S MAINTENANCE

3-1. GENERAL

This chapter provides the Operator's maintenance instructions and procedures for Data Processing Set AN/UYK-64 (V). Operator Maintenance is limited to cleaning and replacing fuses.

3-2. LUBRICATION

No lubrication or lubricants are required.

3-3. CLEANING

The following cleaning procedure is to be performed by the Operator as required.

(1) Remove dust and dirt from exterior surfaces using a clean, lint-free cloth (item 3, appx E).

WARNING

Isopropyl alcohol is extremely flammable; use in well ventilated area away from fire, sparks, or any other heat source. When not in use, keep alcohol container closed.

(2) Remove grease using a clean, line-free cloth (item 3, appx E) soaked with isopropyl alcohol (item 1, appx E). Wipe dry using a clean, lint-free cloth.

(3) Use a bristle brush (item 2, appx E) to remove dirt from hard to reach areas.

(4) Verify that the ETM indicator appears to be operating.

(5) Remove caked-on dirt using a bristle brush (item 2, appx E) soaked with isopropyl alcohol (item 1, appx E). Wipe dry using a clean, lint-free cloth (item 3, appx E).

3-4. REMOVING FUSES

WARNING

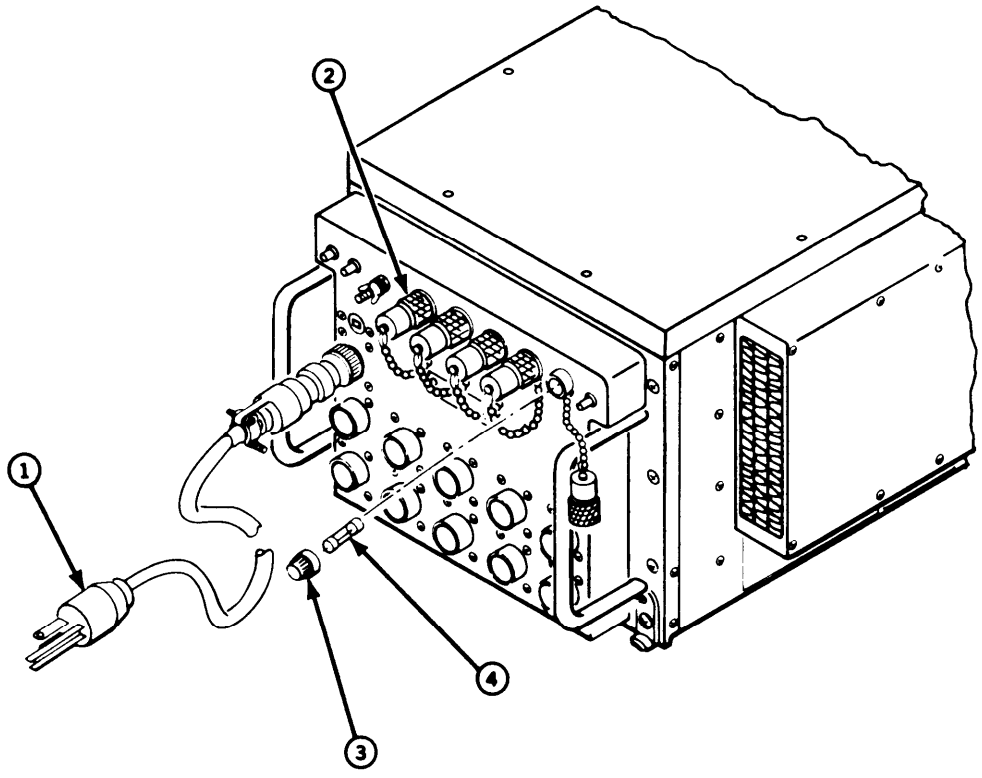
Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

(1) Remove plug (1) from power source.

(2) Unscrew fuseholder cover (2) to the left, then remove cover.

(3) Push fuseholder cap (3) in and to the the left ¼ turn, and remove fuseholder cap (3) with fuse (4).

(4) Remove fuse (4) from fuseholder cap (3).



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3-5. INSTALLING FUSES

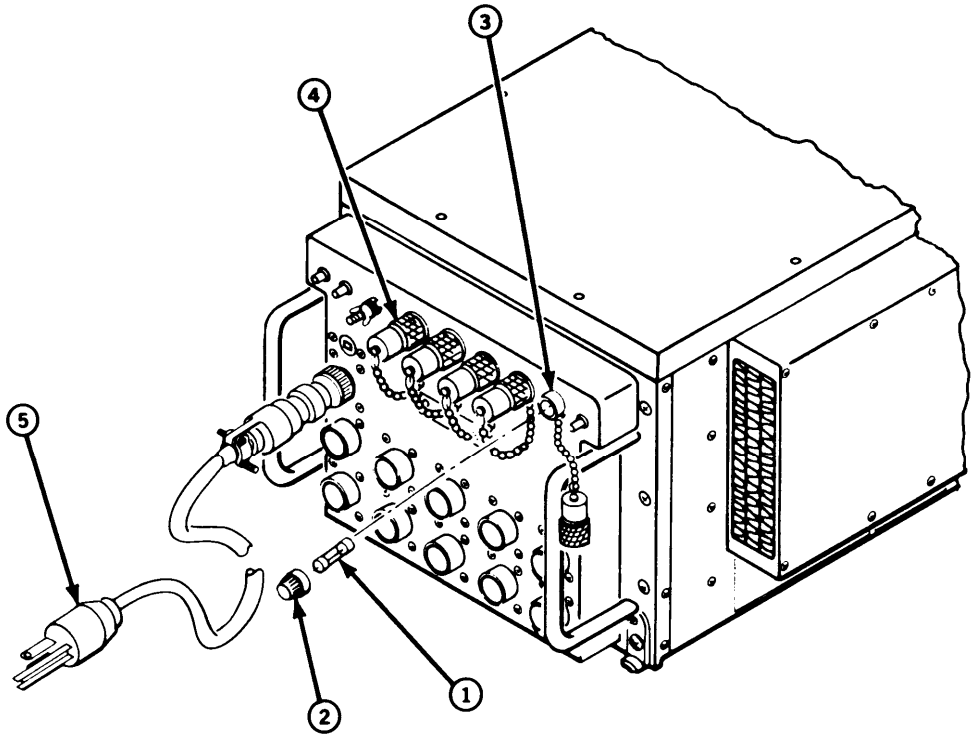
(1) Put fuse (1) in fuseholder cap (2).

(2) Put fuseholder cap (2) with fuse (1) in fuseholder receptacle (3).

(3) Push in on fuseholder cap (2) and turn it to the right until it it is tight.

(4) Install fuseholder cover (4) over fuseholder cap (2).

(5) Connect plug (5) to power source.



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CHAPTER 4

ORGANIZATIONAL MAINTENANCE

Section I. INTRODUCTION

4-1. GENERAL

This chapter provides Organizational maintenance instructions and procedures for Data Processing Set AN/UYK-64 (V). Organizational maintenance is limited to tasks defined in this chapter. The more difficult tasks are referred to higher levels of maintenance.

At the completion of a repair procedure, turn the processor on and repeat the test originally used to detect the problem. This ensures that repairs were accomplished satisfactorily and the unit is operating properly. Refer to paragraph 2-7 for processor turn-on procedures. Instructions for preparation of the unit for storage and shipment are given in chapter 5.

4-2. TOOLS AND TEST EQUIPMENT

Tools and test equipment required for Organizational maintenance of the processor are listed in the Maintenance Allocation Chart (MAC), Appendix B.

4-3. SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

There are no special tools, TMDE, or item of support equipment required at this level of maintenance.

4-4. REPAIR PARTS

Repair parts are listed and illustrated in TM 11-7021-202-20P.

4-5. ORGANIZATIONAL MAINTENANCE TASKS

Following is a list summarizing the maintenance tasks to be performed as required by Organizational maintenance personnel:

- Organizational PMCS
- Troubleshooting
- Equipment removal and replacement
- Cleaning
- Testing after replacements or repairs

Section I. TROUBLESHOOTING

4-6. INTRODUCTION

The processor is a complex piece of electronic equipment. Organizational maintenance personnel perform only those troubleshooting procedures contained within this manual. If a malfunction occurs that is not covered in this manual, or if the listed maintenance action does not correct the trouble, the processor is removed from its mounting and replaced with a functioning spare processor. The defective processor is then referred to higher levels of maintenance for repair.

NOTE

This manual cannot list all malfunctions that might occur, or all tests, inspections, and corrective actions required. If a malfunction is not listed, or is not resolved by the listed corrective actions, notify the shift supervisor.

4-7. USE OF TROUBLESHOOTING FLOWCHARTS

a. Locate the malfunction in the Symptom Index.

b. Note that the troubleshooting flowcharts and procedures are indexed by malfunction/symptom.

c. Review the sample flowchart (fig. 4-1) to become familiar with the proper use of troubleshooting flowcharts.

4-8. SYMPTOM INDEX

Table 4-1 provides an index of probable equipment malfunction symptoms. Use the index to quickly locate applicable troubleshooting flowchart and/or procedures to determine the required corrective action(s).

4-9. TROUBLESHOOTING

a. The first step in troubleshooting the processor is to locate the symptom in the troubleshooting Symptom Index (table 4-1).

b. Next, go to the applicable flowchart or procedure for that symptom.

c. After performing the required troubleshooting and making repairs, observe that upon—application of power to the processor that the BITE self-test is completed successfully, ensuring that repairs have been accomplished properly.

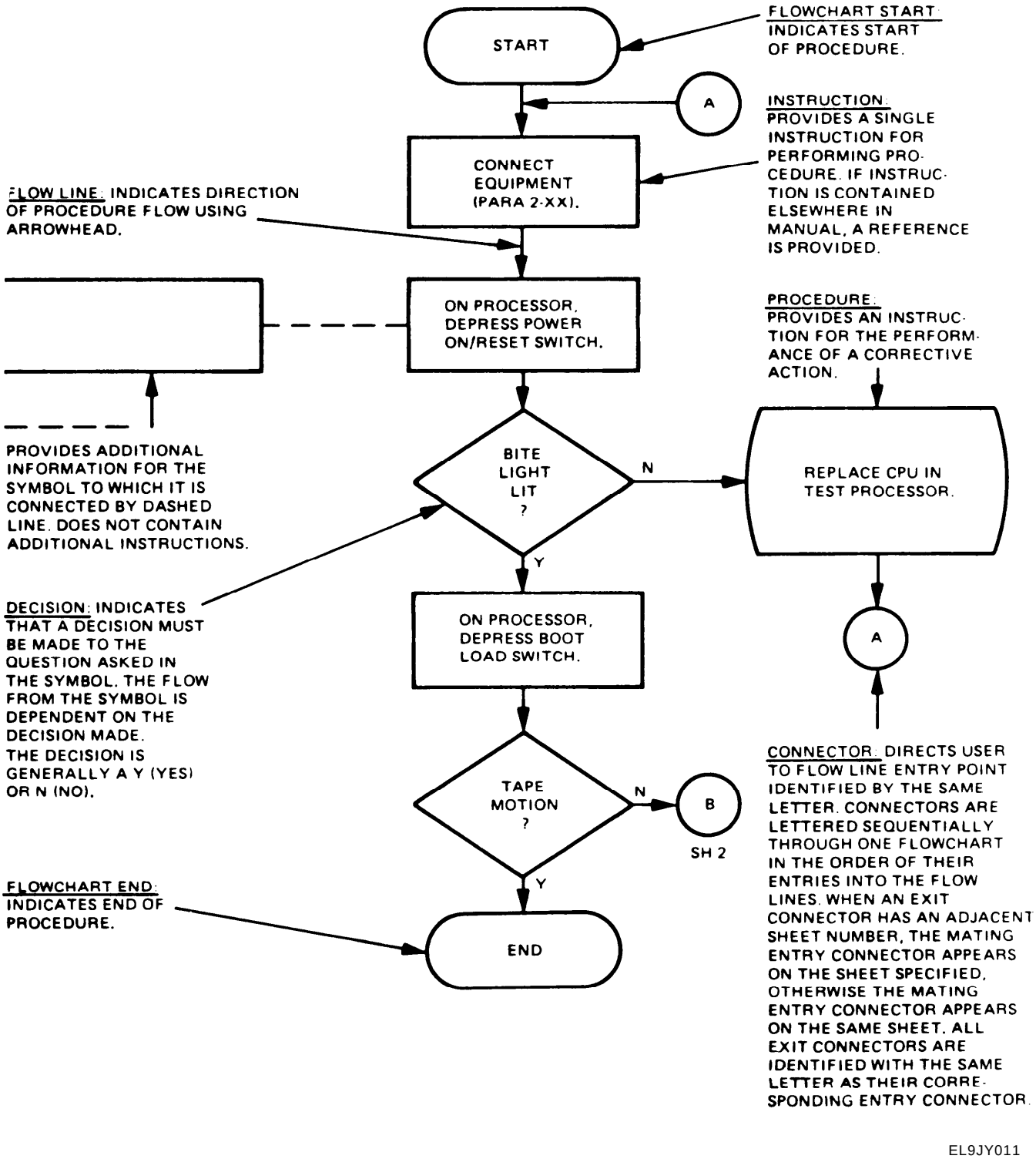


Figure 4-1. How to Use the Flowchart, Sample Flowchart

Table 4-1. Processor Malfunction/Symptom Index

Malfunction/Symptom	Flowchart/Para
1. Smoke and fire.	Paragraph 4-10 a
2. Unit overheating.	Paragraph 4-10 a
3. Noisy blower fan.	Paragraph 4-10 c
4. PWR ON/RESET, BITE/BOOT, BAIT indicators not lit.	Flowchart (1)
5. PWR ON/RESET indicator not lit.	Paragraph 4-10 d
6. BITE/BOOT indicator not lit.	Flowchart (2)
7. BAIT indicator not lit.	Paragraph 4-10 e
8. RUN/RESET indicator won't light.	Flowchart (3)
9. Defective ETM indicator.	Paragraph 4-10 f
10. Program won't load.	Paragraph 4-10 g
11. Processor does not accept data.	Paragraph 4-10 h
12. Processor does not output data.	Paragraph 4-10 i
13. Processor keeps blowing fuses.	Paragraph 4-10 j

d. The following general rules apply while performing troubleshooting:

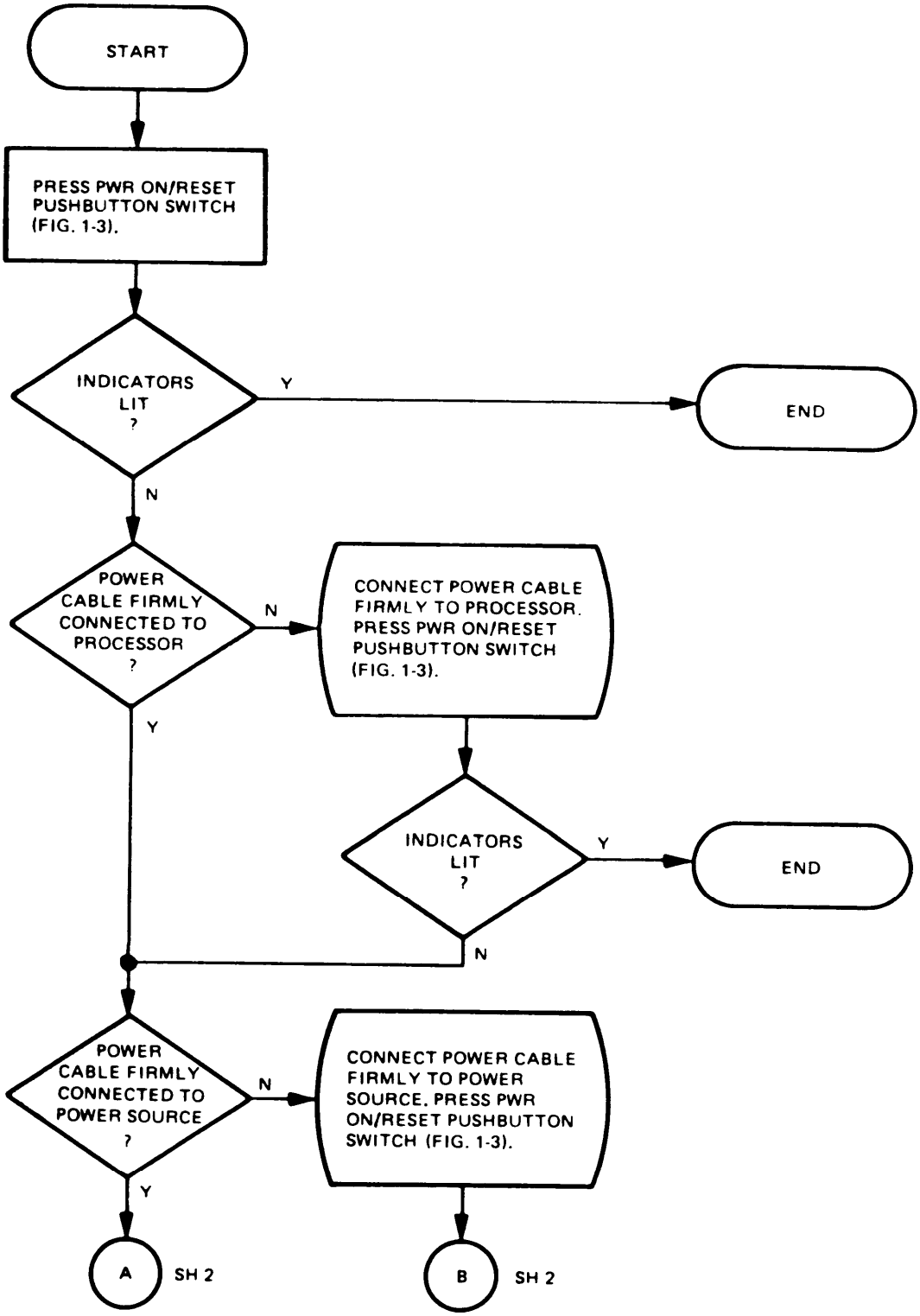
(1) Follow the troubleshooting flowcharts and procedures in the order indicated by the flow arrows or sequence of procedural steps.

(2) Perform only one instruction at a time.

(3) Start at the beginning of the troubleshooting flowchart or procedure. Do not start in the middle.

TROUBLESHOOTING FLOWCHART 1

PWR ON/RESET, BITE/BOOT, AND BATT INDICATORS NOT LIT (SHEET 1 OF 3)



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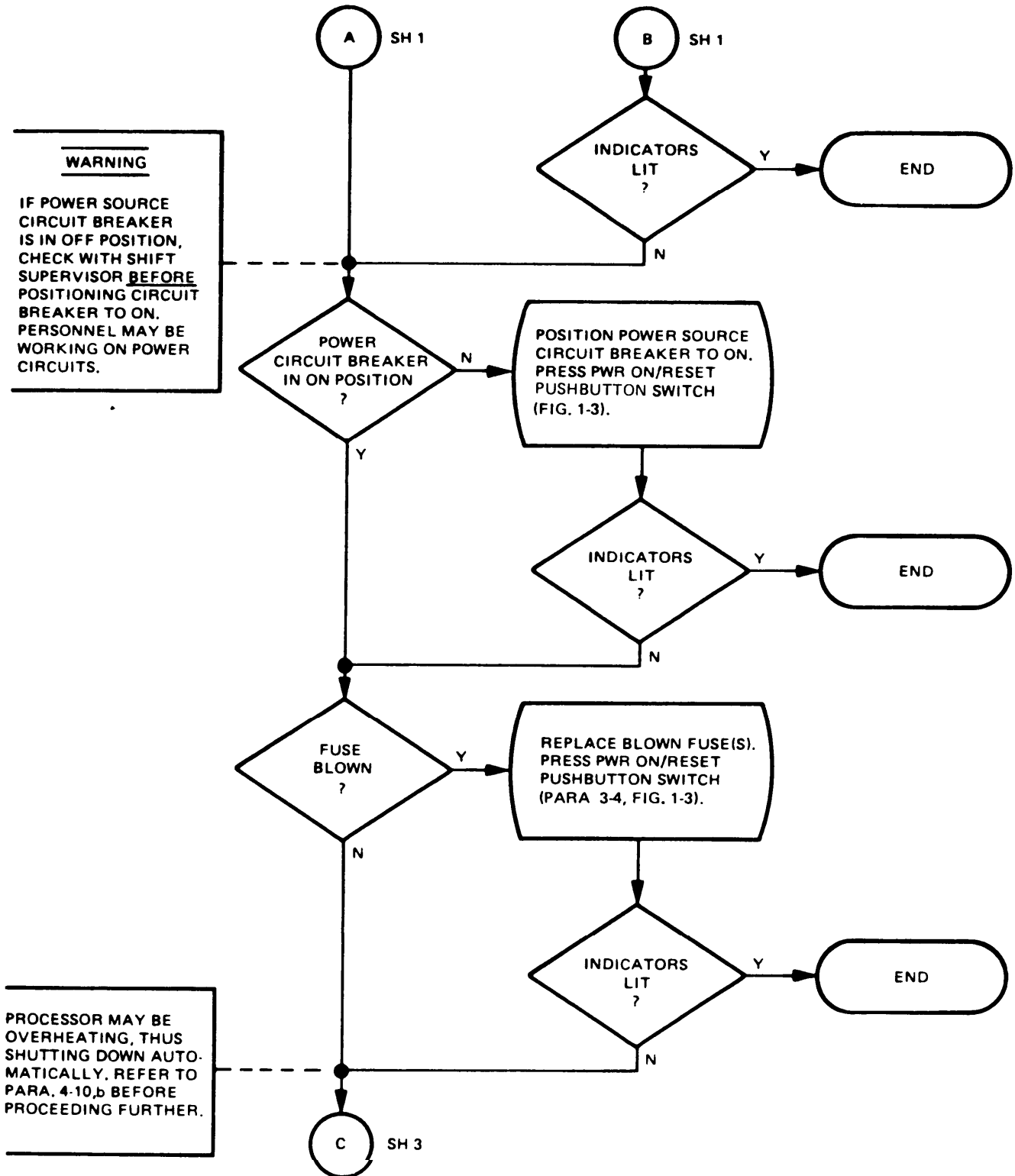
TROUBLESHOOTING FLOWCHART 1 — Continued

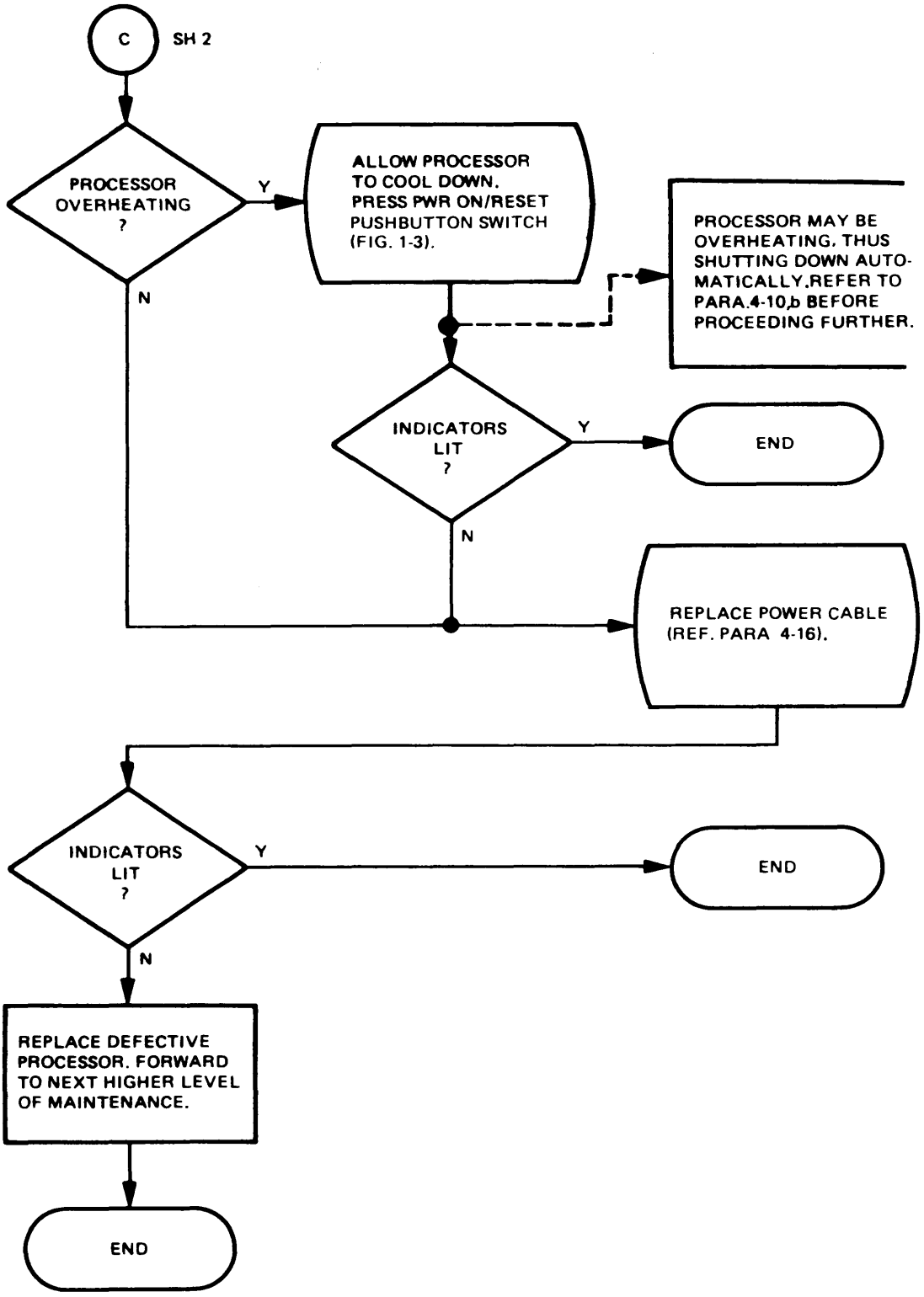
PWR ON/RESET, BITE/BOOT, AND BATT INDICATORS NOT LIT (SHEET 2 OF 3)



EL9JY013

TROUBLESHOOTING FLOWCHART 1 — Continued

PWR ON/RESET, BITE/BOOT, AND BATT INDICATORS NOT LIT (SHEET 3 OF 3)



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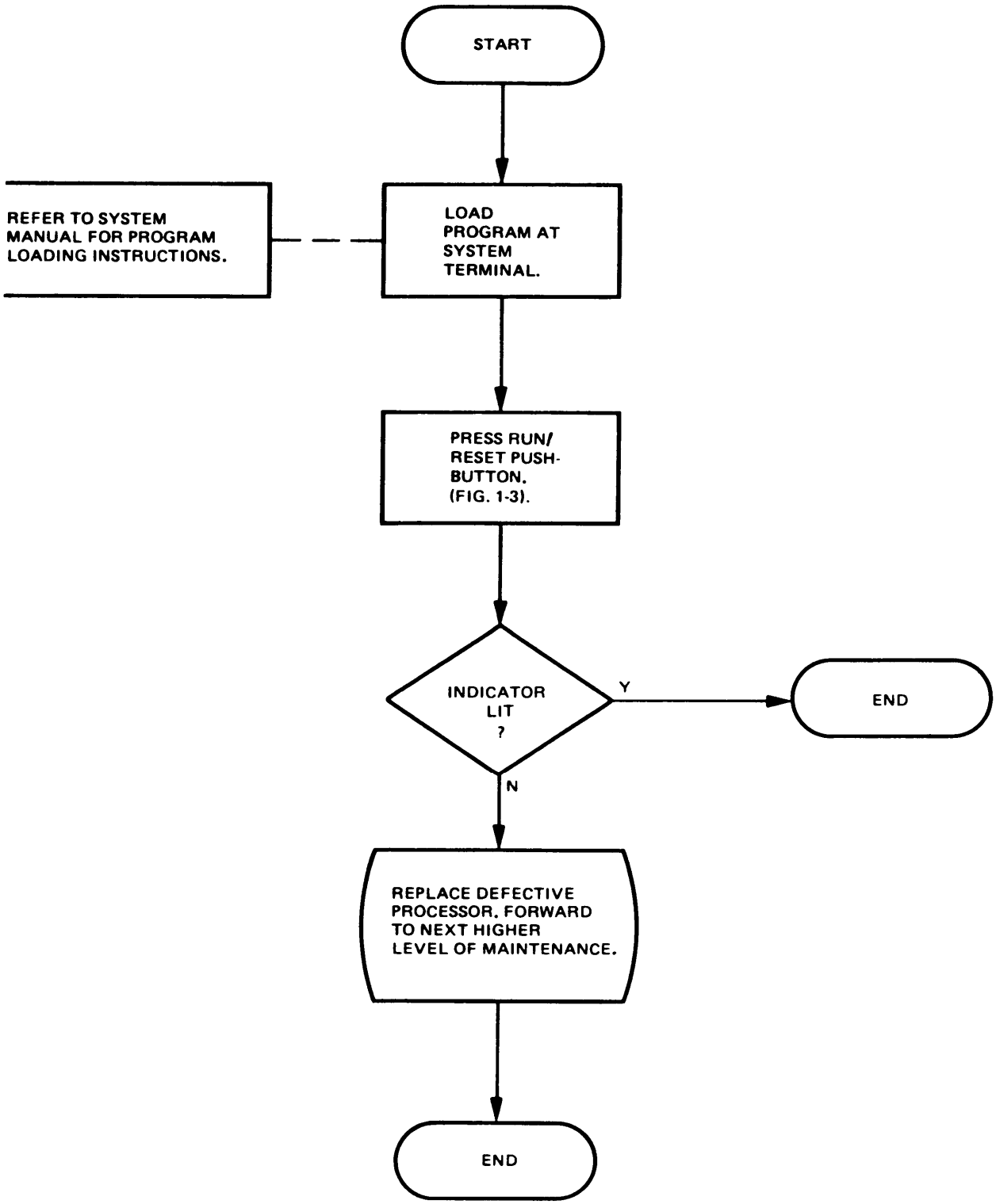
TROUBLESHOOTING FLOWCHART 2

BITE/BOOT INDICATOR NOT LIT (SHEET 1 OF 1)



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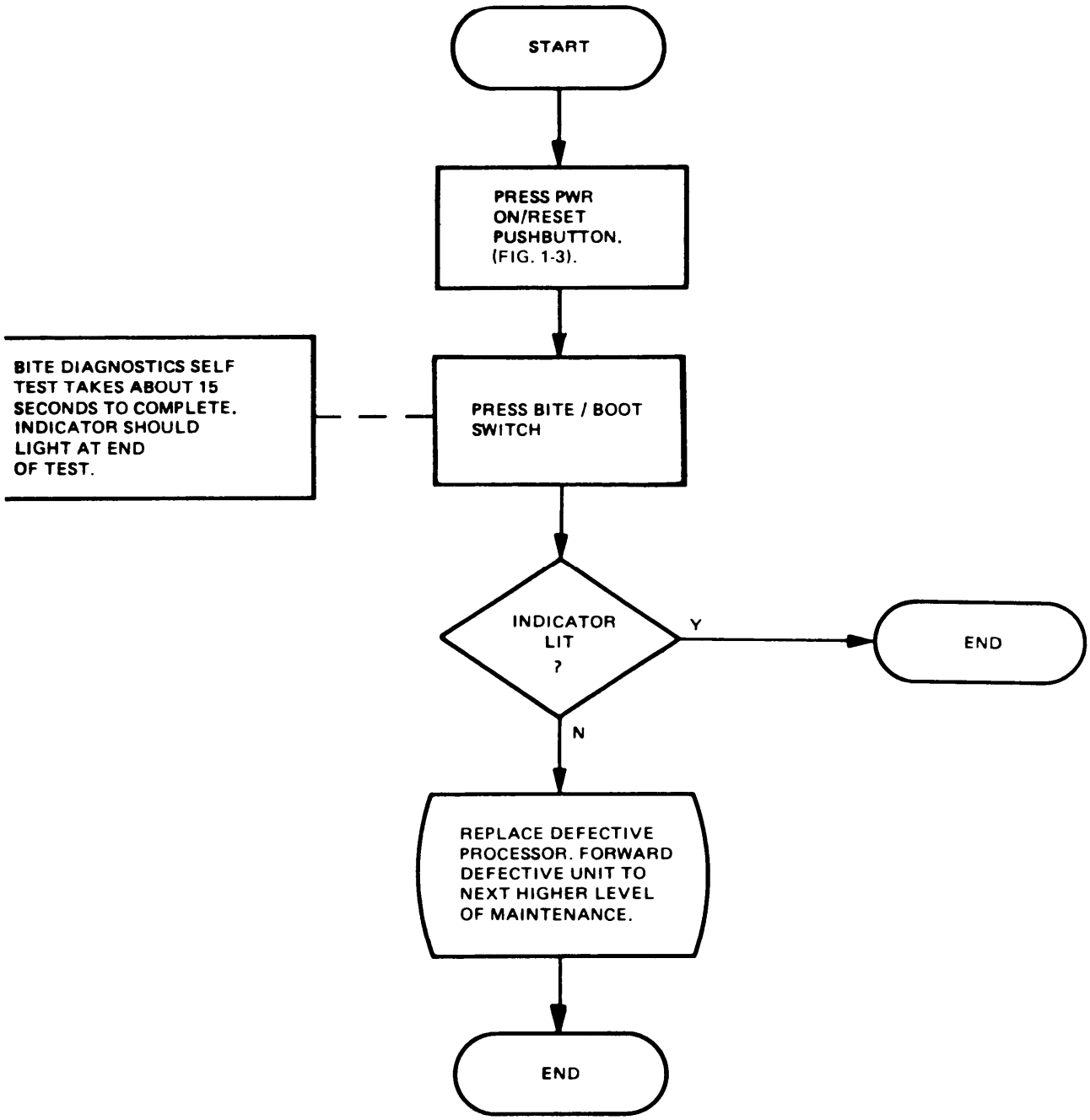
TROUBLESHOOTING FLOWCHART 3

RUN/RESET INDICATOR NOT LIT (SHEET 1 OF 1)



EL9JY016

4-10. TROUBLESHOOTING PROCEDURES

The following procedures provide the user with troubleshooting instructions and corrective action procedures required when maintaining the processor.

WARNING

HIGH VOLTAGE is used in this equipment. **DEATH ON CONTACT** may result if safety precautions are not observed.

CAUTION

DO NOT replace defective processor with a spare unit until the cause of the smoke and fire has been determined and all power cabling has been checked out as operational and safe.

a. Smoke and Fire. If smoke and fire are encountered when operating the processor, immediately disconnect the processor from the power source.

b. Unit Overheating. Overheating of the processor can be caused by a number of things (e. g., restricted airflow around the unit, defective heat exchanging within the unit itself, defective power supply, etc.). However, an overheated condition is not always immediately obvious to the Operator or maintenance personnel. Whenever the unit becomes overheated, the unit's power supply will automatically shut down the processor. The symptom will appear as a malfunction in the prime power circuits, normally resulting in replacement of the defective unit. Refer to the PWR ON/RESET, BATT, and BITE/BOOT Indicators Not Lit troubleshooting flowchart. Once the unit has had time to cool off, it will return to an operational state. Depressing the PWR ON/RESET pushbutton switch will bring the unit back on line.

If the cause of the overheating has not been located and corrected, the processor will continue to operate only as long as it takes to become overheated. Then, once again, it will automatically shut down. Therefore, the only real clue that the unit may be overheating is that it keeps shutting down, and after a period of time has passed and the processor has had time to cool down, it returns to an operative condition without repairs being performed.

NOTE

Overheating of the unit is not the only possible cause of the symptom described in the above paragraphs. If the problem persists after airflow restrictions are cleared, the problem is not within the scope of this manual.

It is very important that the Operator and maintenance personnel ensure that the environment around the processor is such that the airflow through and around the unit is not restricted or the air temperature is above requirements (table 1-2).

c. Noisy Blower Fan. In the event that the units blower fan becomes noisy, the processor is removed and replaced with an operational spare (para 4-14).

d. PWR ON/RESET Indicator Not Lit. If the PWR ON/RESET indicator won't light, replace the defective processor with an operational spare (para 4-14).

e. BATT Indicator Not Lit. If the BAIT indicator on a semiconductor-based processor won't light and the PWR ON/RESET is lit, the repair activity is beyond the scope of this manual. Replace the defective processor with an operational spare (para 4-14).

NOTE

The ETM indicator can be checked by observing the movement of the flag between the first and second digits.

f. Defective ETM Indicator. A daily visual inspection of the Elapsed Time Meter (ETM) will show if the meter is not functioning properly. When the meter is not operating properly, replace the processor with an operative spare unit (para 4-14).

g. Program Won't Load. Failure of the program to load may be caused by a number of things. The most probable cause is in the loading itself (i. e., improper address, improper/incomplete equipment configuration, etc.). Refer to the system manual for proper loading instructions. Another probable cause is the processor itself. If the cause is the processor, replace the processor with a spare operative unit (para 4-14).

h. Processor Does Not Accept Data. Replace the defective processor with an operational spare unit (para 4-14).

i. Processor Does Not Output Data. Replace the defective processor with an opertional spare unit (para 4-14).

j. Processor Keeps Blowing Fuses. Replace the processor with an operational spare unit (para 4-14).

Section III. ORGANIZATIONAL MAINTNANCE PROCEDURES

4-11. INTRODUCTION

This section provides the Organizational Maintenance PMCS procedures for the processor.

4-12. ORGANIZATIONAL PMCS

Table 4-2 provides the PMCS to be performed at the organizational maintenance level.

Table 4-2. Organizational PMCS
W = Weekly

Item No.	Interval W	Item To Be Inspected/ Procedure
1	●	**FAN:** Vacuum housing.
2	●	**AIR DUCTS:** Vacuum from end.
3	●	**FUSES:** Remove fuses and check for proper ratings.
4	●	**PUBLICATIONS:** Check for completeness of, and current changes to publications.

Section IV. REMOVAL AND REPLACEMENT PROCEDURES

4-13. INTRODUCTION

Following are procedures for removing and replacing the processor and its components. Refer to the system manual for system configuration removal and replacement requirements.

WARNING

The processor is a heavy piece of equipment. Always use three technicians when moving or lifting the unit to prevent injury to personnel.

4-14. REMOVING PROCESSOR

a. If the processor is rack mounted, extend the unit out of the rack to its fullest position.

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

b. Disconnect processor's power cable from prime power source (para 4-16).

c. Disconnect all I/O cabling from the processor (para 4-18). If applicable, disconnect all ground straps/cables. Place dust caps over all connectors on the unit and disconnected cable connectors.

WARNING

The processor is a heavy piece of equipment. Always use three technicians when moving or lifting the unit to prevent injury to personnel.

NOTE

If the processor is positioned in a counter-top (free-standing) configuration, the performance of step d below is not required.

d. Lift unit out of the rack assembly and set it on a clean workbench or maintenance cart.

e. Complete applicable documentation and tagging before forwarding the unit to the next higher level of maintenance (para 1-3).

f. Package and pack the defective unit in accordance with instructions provided in chapter 5.

g. Forward defective unit to Direct Support Maintenance.

4-15. **INSTALLING PROCESSOR**

WARNING

The processor is a heavy piece of equipment. Always use three technicians when moving or lifting the unit to prevent injury to personnel.

a. Remove unit from the packing and packaging in which it was received. File documents (i. e., reports, tags, etc.) that accompanied the unit.

b. Remove dust caps from the connectors on the unit. Remove dust caps from the cables to be connected up to the unit.

c. Position the processor in its operating location (rack-mount or counter-top configuration).

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

d. Connect power cable to processor (para 4-17).

e. Connect I/O cabling to the processor in accordance with the cabling diagram requirements listed and shown in the system manual (para 4-19). If applicable, connect ground strapping/cabling in accordance with requirements of system manual.

f. Ensure that airflow around installed unit is not restricted in any way.

g. Connect power cable to prime power source. Refer to paragraph 2-7 for turn-on procedures.

h. Perform Preventive Maintenance Checks and Services (PMCS). Refer to chapter 2.

i. Bring the unit on line with the system in accordance with the instructions contained in the system manual.

4-16. REMOVING POWER CABLE

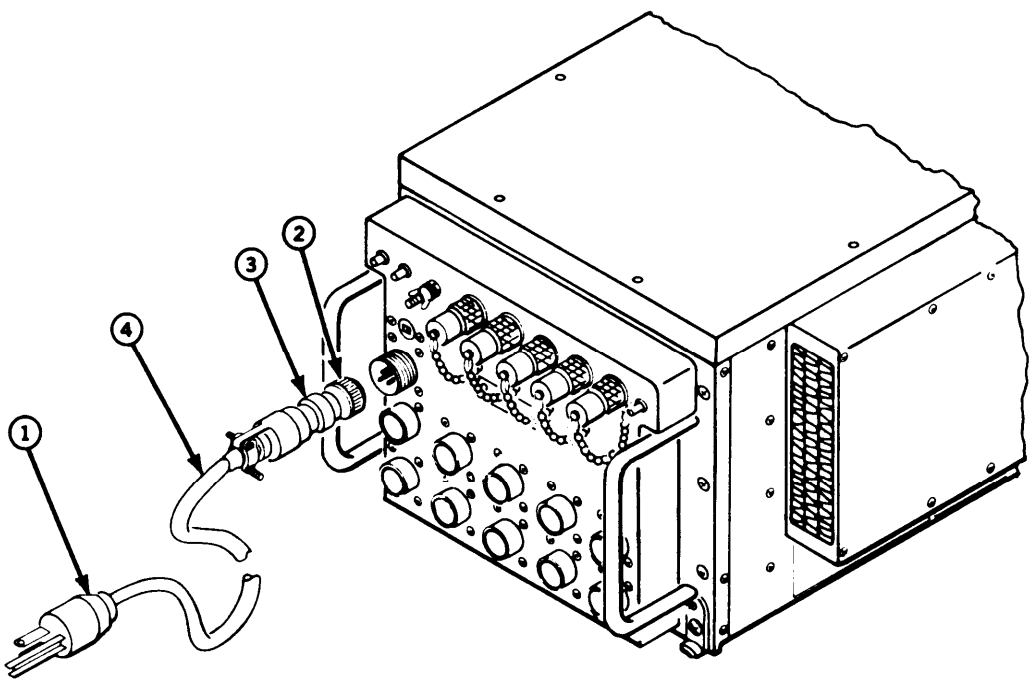
WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Remove plug (1) from power source.

b. Unscrew knurled nut (2) to left and unplug connector (3).

c. Remove power cable (4).



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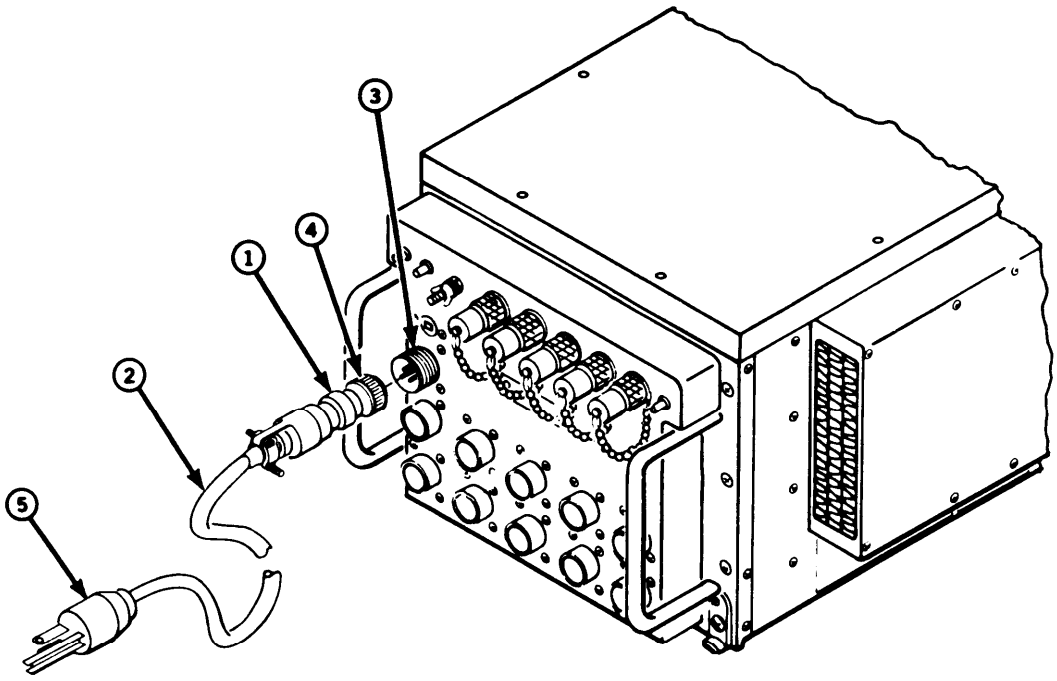
4-17. INSTALLING POWER CABLE

a. Aline slot of connector (1) on power cable (2) with key on power connector (3).

b. Plug connector (1) into power connector (3) and screw on knurled nut (4) to the right until tight.

c. Connect plug (5) to power source.



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4-18. REMOVING I/O SIGNAL CABLES

WARNING

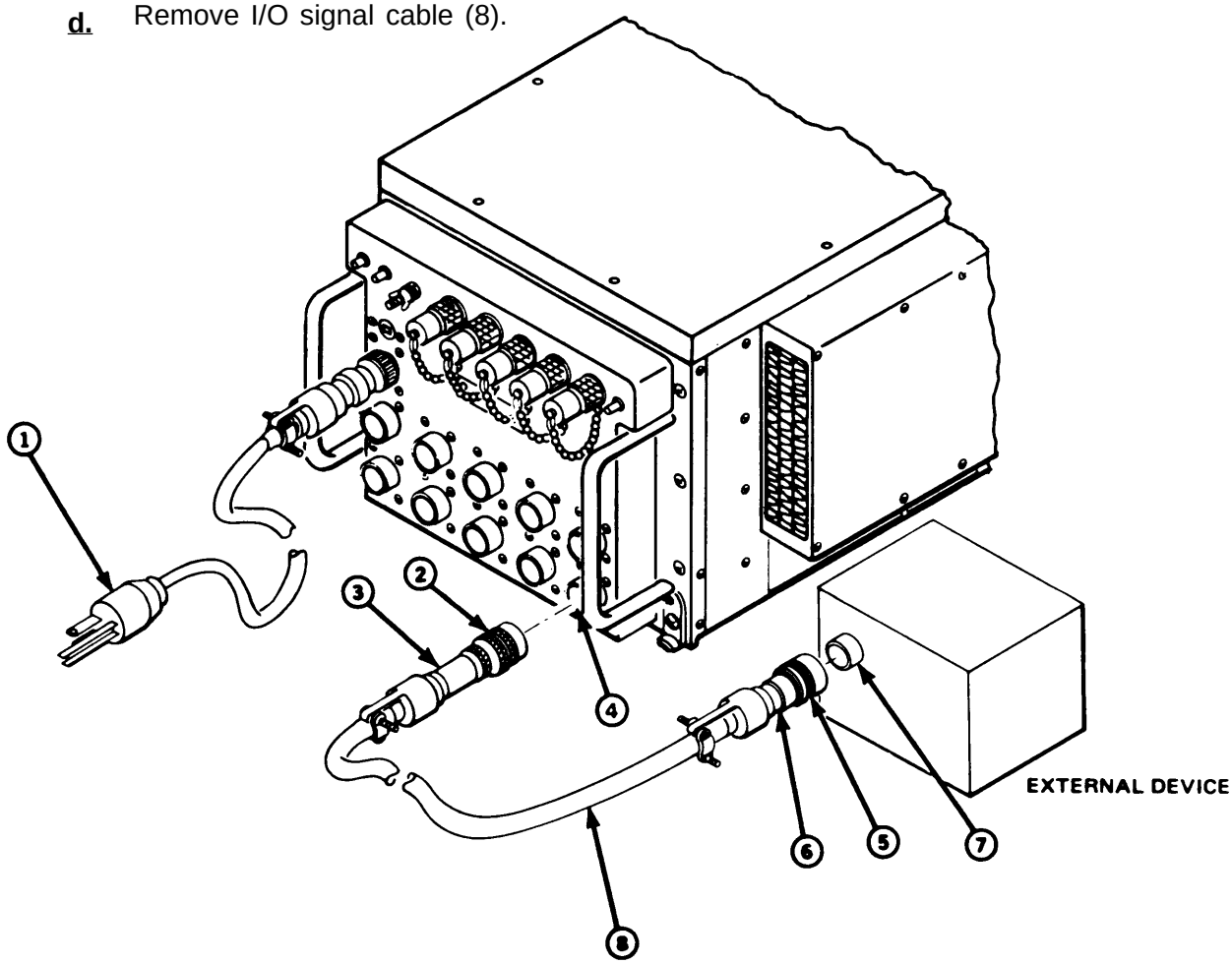
Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

a. Disconnect power cable plug (1) from power source.

b. Turn knurled ring (2) to the left and unplug I/O cable connector (3) from processor connector (4).

c. Turn knurled ring (5) to the left and unplug I/O cable connector (6) from connector (7) on the external device.

d. Remove I/O signal cable (8).



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4-19. INSTALLING I/O SIGNAL CABLES

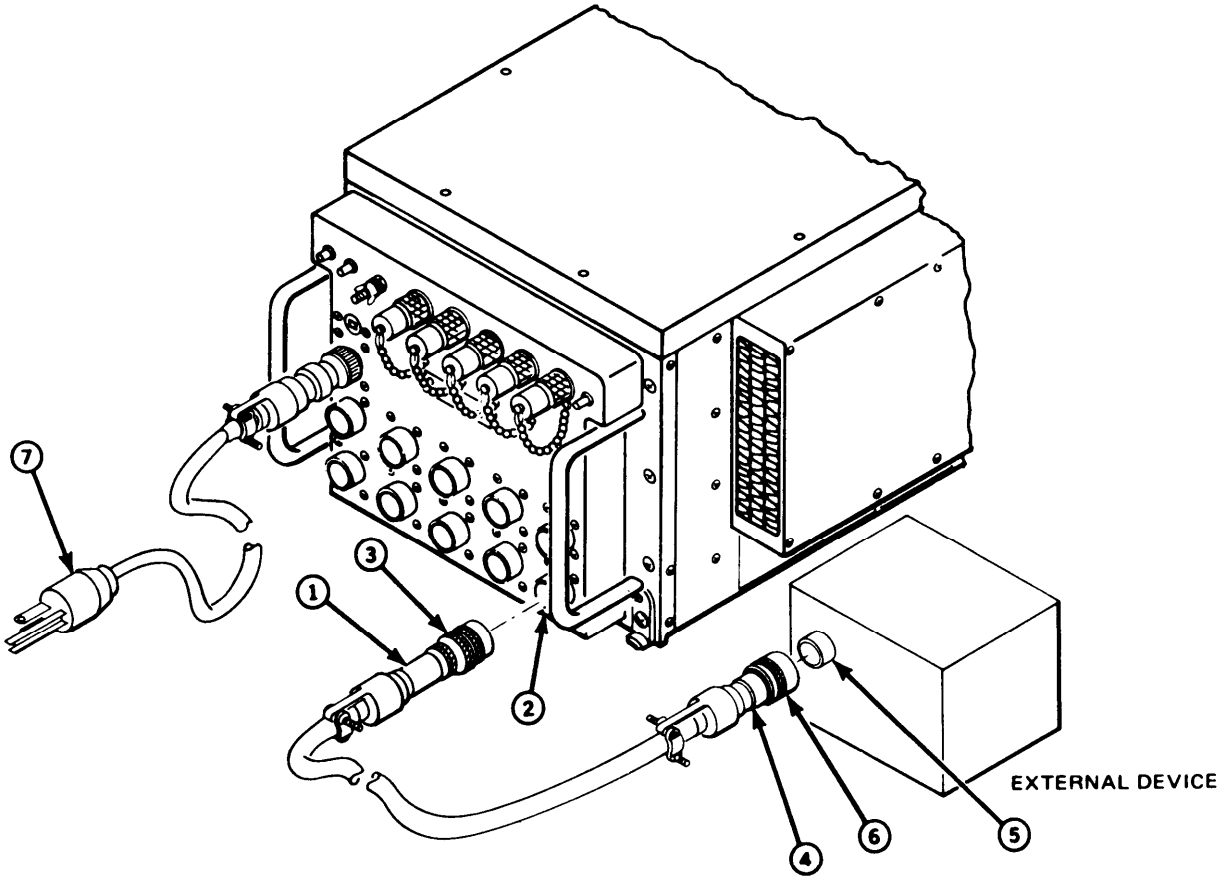
a. Aline keys on I/O cable connector (1) with slots on processor I/O connector (2).

b. Plug connector (1) into connector (2). Turn knurled ring (3) to the right until it clicks in place.

c. Aline keys on I/O cable connector (4) with slots on external device connector (5).

d. Plug connector (4) into connector (5). Turn knurled ring (6) to the right until it clicks in place.

e. Connect power cable (7) to power source.



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4-20. CLEANING

a. **Tools and Materials.** The following tools and materials are required when cleaning the processor:

- Lint-free cloths (item 3, appx E)
- Soft-bristle brush (item 2, appx E)
- Dishwashing compound or detergent (item 4, appx E)
- Alcohol isopropyl (item 1, appx E)
- Vacuum cleaner with attachments.

b. **Cleaning.** Cleaning of the processor is limited to the following activities:

WARNING

Turn off power before working on equipment. Failure to do so can cause serious injury to personnel.

Use alcohol only in well-ventilated area away from fire, sparks, or any other heat source that might ignite it.

(1) Dusting of all external surfaces.

(2) Wiping off smudges and deposits of foreign matter.

(3) Clearing debris off of the processor and from the immediate area around the processor.

(4) Vacuuming dust/debris from the air inlet ducts, and from the blower assembly at the rear of the processor.

4-21. TESTING AFTER REPLACEMENTS OR REPAIRS

Upon completion of all replacements and/or repairs, the processor is tested as follows:

WARNING

The processor is a heavy piece of equipment. Always use three technicians when moving or lifting the unit to prevent injury to personnel.

(1) Place the processor in a stand-alone configuration on a workbench with no I/O cabling attached. Then apply power to the processor (para 2-7) and ensure that the BITE self-test runs without errors (para 2-7).

NOTE

If at any point in the procedure the processor fails to operate properly, refer to chapter4, Section II and perform the required troubleshooting.

(2) Remove power to the unit by disconnecting the power cable connector from the power source.

(3) Position the processor into its normal operating location (stand-alone or rack mounting), and connect I/O cables, connect ground strapping if applicable, and finally connect the power cable connector to the power source.

(4) Once again, verify a successful BITE self-test.

CHAPTER 5

PACKING FOR SHIPMENT OR STORAGE

5-1 . INTRODUCTION

This section provides procedures for packing Data Processing Set AN/UYK-64 (V). Material used for packing is listed in the Expendable Supplies and Materials List (ESML), appendix D. Instructions reference each item in the ESML as it is used.

5-2. PREPARATION FOR STORAGE OR SHIPMENT

Prior to packing the processor for shipment or storage, perform routine Preventive Maintenance Checks and Services (PMCS). Refer to paragraph 1-4. If the processor is being forwarded to a higher level of maintenance for repairs, prepare the required equipment failure report in accordance with paragraph 1-3.

5-3. PROCESSOR PACKAGING AND PACKING

When packaging and packing the processor for shipment or storage, see figure 5-1 and perform each of the following steps:

NOTE

Packaging and packing the processor intact is not recommended. The units power supply and printed-circuit boards (PCB) should be removed and packaged and packed in separate containers. However, disassembly of the processor is beyond the scope of this manual.

a. Install two desiccant bags (item 5, appx E) in a plastic bag (item 6, appx E).

WARNING

The processor is a heavy piece of equipment. Always use three technicians when moving or lifting the unit to prevent injury to personnel.

b. Place the unit in the plastic bag (item 6, appx E).

c. Place all maintenance forms and tags in the plastic bag with the unit and seal the plastic bag with tape (item 7, appx E).

d. Place the bag containing the unit in a polyurethane foam container (item 8, appx E).

e. Place the polyurethane cover (item 10, appx E) on the container and seal with pressure sensitive tape (item 9, appx E).

f. Wrap the polyurethane container with a barrier material (item 11, appx E).

g. Secure the wrapping material with tape (item 7, appx E).

h. Complete shipping label (item 14, appx E) and affix it to the carton (item 12, appx E).

i. Complete shipping forms, place forms in packing list envelope (item 13, appx E), and affix the envelope to the carton as shown.

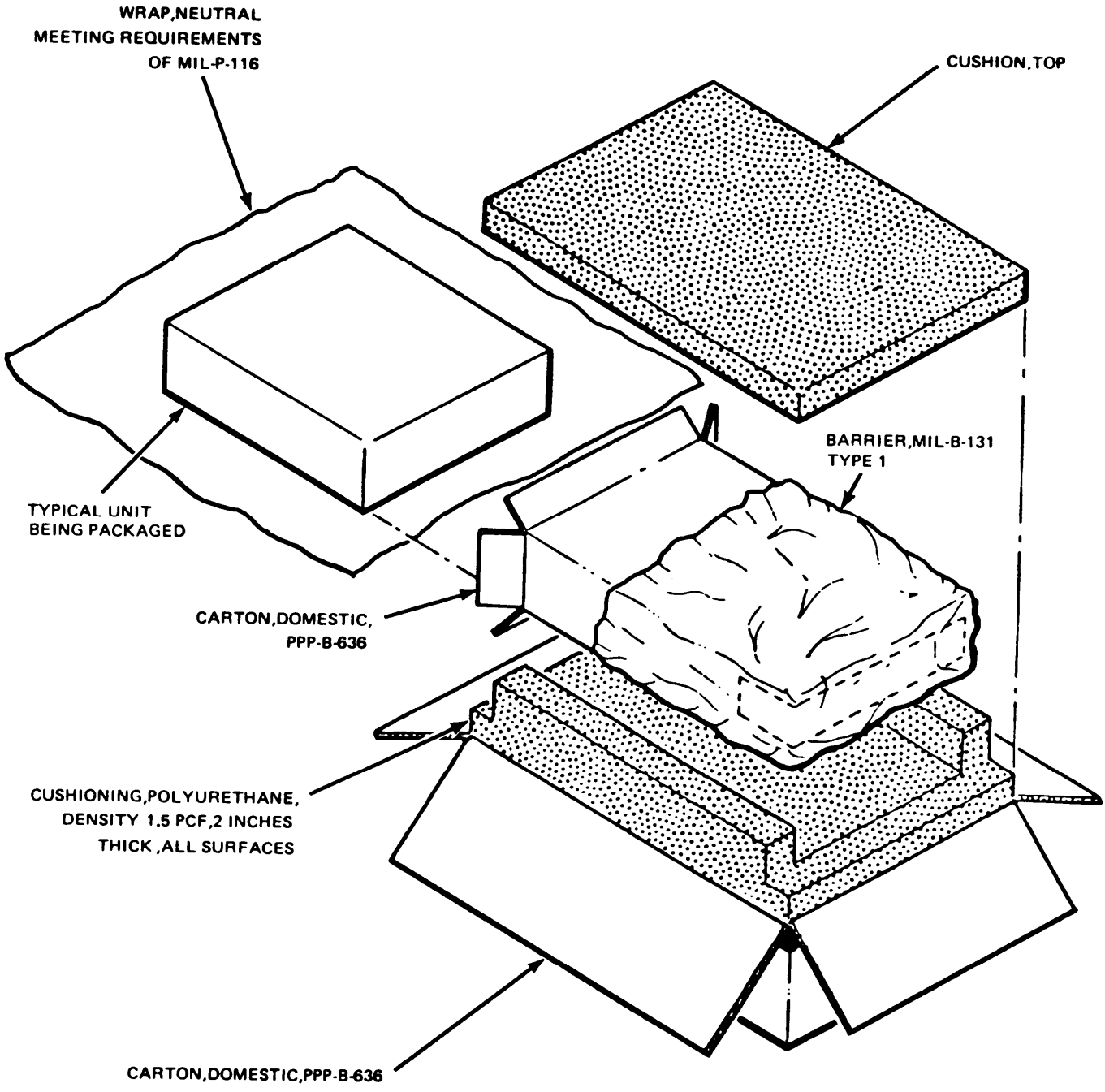

Figure 5-1. Packing a Typical Unit

APPENDIX A

REFERENCES

A-1. SCOPE

This appendix lists all forms and technical publications referenced in this manual.

A-2. FORMS

Recommended Changes to Equipment Technical Publications . . . . . DA Form 2028-2

Recommended Changes to Publications and Blank Forms . . . . . DA Form 2028

Equipment Inspection and Maintenance Work Sheets . . . . . DA Form 2404

Maintenance Request . . . . DA Form 2407

Equipment Log Assembly (Records).. . . . . .DA Form 2408

Equipment Daily Log . . . . DA Form 2408-1

Discrepancy in Shipment Report . . . . . .SF 361

Report of Discrepancy . . . . . .SF 364

A-3. TECHNICAL BULLETINS None

A-4. TECHNICAL MANUALS

Organizational Maintenance, Repair Parts and Special Tools List,Data Processing Set AN/UYK-64 (V) . . . . . TM 11-7021-202-20P

Packaging of Material Preservation . . . . TM 38-230-1

Packaging of Material;Packing. . . . . .. TM 38-230-2

Administrative Storage of Equipment . . . . TM 740-90-1

Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command) . . . . . TM 750-244-2

First Aid for Soldiers . . . . FM 1-11

A-5. SUPPLY BULLETINS

Preservation, Packaging, and Packing Materials, Supplies, and Equipment Used By the Army . . . . . .SB 38-100

Common Table of Expendable Items . . . . . .CTA 50-970

A-6. PAMPHLETS

Consolidated lndex of Army Publications and Blank Forms . . . . . DA PAM 310-1

The Army Maintenance Management System (TAMMS) . . . . . DA PAM 738-750

A-7. ARMY REGULATIONS

Dictionary of United States Army Terms . . . . . .AR 310-25

Catalog of Abbreviations and Brevity Codes . . . . . .AR 310-50

Classification, Reclassification Maintenance, insurance and Reporting of Maintenance Training Aircraft . . . . . .AR 700-42

Reporting of Transportation Discrepancies in Shipments . . . . . .AR 55-38

A-8. FEDERAL SPECIFICATIONS AND STANDARDS

Box, Wood, Nailed, and Locked Corners PPP-B-621

Box, Shipping, Fiberboard PPP-T-636

Tape, Gummed, Paper, Reinforced, and Plain, for Sealing and Servicing PPP-T-45

APPENDIX B

MAINTENANCE ALLOCATION CHART FOR PROCESSING SET AN/UYK-64(V)

Section I. INTRODUCTION

B-1. GENERAL

This appendix provides a summary of the maintenance operations for the Processor. It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

B-2. MAINTENANCE FUNCTION

Maintenance functions will be Iimited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.

b. Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition, i.e., to clean (decontaminate), to preserve, to drain, to paint, or to replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.

d. Adjust. To maintain, within prescribed limits, by bringing into proper or exact position, or setting the operating characteristics to the specified parameters.

e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Install. The act of emplacing, seating, or fixing into position an item, part, module (component or assembly) for an unserviceable counterpart.

h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counterpart.

i. **Repair.** The application of maintenance services (inspect, test, service, adjust, align, calibrate, replace) or other maintenance actions (welding, grinding, riveting, straightening, facing, remachining, or resurfacing) to restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly), end item, or system.

j. Overhaul. That maintenance effort (service/action) necessary to restore an item to a completely serviceable/operational condition as prescribed by maintenance standards (i.e., DMWR) in appropriate technical publications. Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuiid. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of material maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipments/components.

B-3. COLUMN ENTRIES

a. Column 1, Group Number. Column 1 lists group numbers, the purpose of which is to indentify components, assemblies, subassemblies, and modules with the next higher assembly.

b. Column 2, Component/Assembly. Column 2 contains the noun name of components, assemblies, subassemblies, and modules for which maintenance is authorized.

c. Column 3, Maintenance Functions. Column 3 lists the functions to be performed on the item listed in column 2. When items are listed without maintenance functions, it is solely for purpose of having the group numbers in the MAC and RPSTL coincide.

d. Column 4, Maintenance Category. Column 4 specifies by the listing of a “worktime” figure in the appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in column 3. This figure represents the active time required to perform that maintenance function at the indicated category of maintenance. If the number of complexity of the tasks within the listed maintenance function vary at different maintenance categories, appropriate “worktime” figures will be shown for each category. The number of task-hours specified by the “worktime” figure represents the average time required to restore an item (assembly, subassembly, component, module, end item, or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time, and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. Subcolumns of column 4 are as follows:

C Operator/Crew

O Organization

F Direct Support

H General Support

D Depot

e. Column 5, Tools and Equipment. Column 5 specifies by code, those common tool sets, (not individual tools) and special tools, and support equipment required to perform the designated function.

f. Column 6, Remarks. Column 6 contains an alphabetic code which leads to the remark in Section IV, Remarks, which is pertinent to the item opposite the particular code.

B-4. TOOL AND TEST EQUIPMENT REQUIREMENTS (SECTION III)

a. Tool or Test Equipment Reference Code. The numbers in this column with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool or test equipment for the maintenance functions.

b. Maintenance Category. The codes in this column indicate the maintenance category allocated the tool or test equipment.

c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

d. National/NATO Stock Number. This column lists the National/NATO stock number of the specific tool or test equipment.

e. Tool Number. This column lists the manufacturer's part number of the tool followed by the Federal Supply Code for manufacturers (5-digit) in parentheses.

B-5. REMARKS (SECTION IV)

a. Reference Code. This code refers to the appropriate item in Section II, Column 6.

b. Remarks. This column provides the required explanatory information necessary to clarify items appearing in Section II.

SECTION II. MAINTENANCE ALLOCATION CHART
FOR
PROCESSING SET AN/UYK-64(V)

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQPT	(6) REMARKS
			C	O	F	H	D		
00	AN/UYK-64 Data Processor Set (V)1 Through (V)4X	Inspect		0.1					
		Replace		0.5				1	E
		Test			0.5			3,4,5	A,B
		Replace			0.1			1,6	
		Repair			4.0			2,4,7	
		Test				2.0		4,9	G
		Repair				4.0		1,2,4	G
		Overhaul					32.0	Depot Facilities	
01	Processor Chassis (Semi) (V)1, (V)1X and (V)3, (V)3X Only	Inspect			0.5			4,8	
		Replace			0.1			1	
		Repair			2.0			2,8	
		Test				1.0		2,8	G
		Repair					4.0	Depot Facilities	
0101	Processor Motherboard (Semi) (V)1, (V)1X and (V)3, (V)3X Only	Test			2.0			4,8	C
		Test				2.0		4,8	F,G
		Repair				4.0			D
		Replace					4.0	Depot Facilities	
010101	Front Panel Assembly (Semi) (V)1, (V)1X and (V)3, (V)3X Only	Inspect		0.1					
		Test				1.0		4,8	F,G
		Repair				1.0		4,7	G
		Replace				0.5		1,4,7	G
0102	EMI Filter (AC) (3883) (V)1, (V)2, (V)3, (V)4 Only	Inspect			0.1			1,4	E
		Replace			0.5			1	K
02	Processor Chassis (Core) (V)2, (V)2X and (V)4, (V)4X Only	Inspect			0.5			4,8	
		Replace			0.1			1	
		Repair			2.0			2,8	
		Test				1.0		2.8	G
		Repair					4.0	Depot Facilitates	
0201	Processor Motherboard (Core) (V)2, (V)2X and (V)4, (V)4X Only	Test			2.0			4,8	C
		Test				2.0		4,8	F,G
		Repair				4.0			D
		Replace					4.0	Depot Facilities	
020101	Front Panel Assembly (Core) (V)2, (V)2X and (V)4, (V)4X	Inspect		0.1					
		Test				1.0		4,8	F,G
		Repair				1.0		4,7	G
		Replace				0.5		1,4,7	G
0202	EMI Filter (DC) (3884) (V)1X, (V)2X, (V)3X and {V)4X Only	Inspect			0.5			4	E
		Replace			0.5			1	K
03	CPU - Board Set (5711) (V)1 Through (V)2X Only	Test			0.5			3,5	L
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
	CPU - Board Set (5710) (V)3 Through (V)4X Only	Test			0.5			3,5	M
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G

SECTION II. MAINTENANCE ALLOCATION CHART
FOR
PROCESSING SET AN/UYK-64(V) - Continued

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EOPT	(6) REMARKS
			C	O	F	H	D		
0301	CPU– Data Board (5711/5710) (V)1 Through (V)4X	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
0302	CPU-Prom Board (5711 Only) (V)1 Through (V)2X Only	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
	CPU - Prom Board (5719 only) (V)3 Through (V)4X Only	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
0303	CPU - PFP Board (V)1 Through (V)4X	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
0304	CPU - MAP Board (V)1 Through (V)4X	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
04	FPU - Board Set (1751) (V)1 Through (V)2X Only	Test			0.5			3,5	M
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
	FPU - Board Set (1751) (V)3 Through (V)4X Only	Test			0.5			3,5	W
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
0401	FPU - A Board (V)1 Through (V)4X	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
0402	FPU - B Board (V)1 Through (V)4X	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
0403	FPU - C (66) Board (V)1 Through (V)2X	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
	FPU-C(E) Board (V)3 Through (V)4X	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G

SECTION II. MAINTENANCE ALLOCATION CHART
FOR
PROCESSING SET AN/UYK-64(V) - Continued

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY C	O	F	H	D	(5) TOOLS AND EQPT	(6) REMARKS
05	Semiconductor Memory Module (2030) (V)1 Through (V)3X Only	Test			0.5			3,5	
		Replace			0.2			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
06	Semiconductor Memory Error CorrectIon Card (1754) (V)1, (V)1X and (V)3, (V)3X Only	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
07	Semiconductor Memory Controller (1753) (V)1, (V)1X and (V)3, (V)3X Only	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
08	Power Supply (AC) (5617) (V)1, (V)2, (V)3, (V)4 Only	Test			0.5			4	
		Replace			0.1			1	
		Test					1.0	2	I,J
		Repair					4.0	Depot Facilities	
09	Power Unit Assembly Heat Exchanger (AC) (V)1, (V)2, (V)3, (V)4 Only	Test			0.5			4	F
		Replace			0.5			1	
		Repair				1.0		1.4	G
10	Power Supply (DC) (5687) (V)1X (V)2X, (V)3X, (V)4X Only	Test			0.5			4	
		Replace			0.1			1	
		Test					1.0	2	I,J
		Repair					4.0	Depot Facilities	
11	Power Unit Assembly Heat Exchanger (DC) (V)1X, (V)2X, (V)3X, (V)4X Only	Test			0.5			4	F
		Replace			0.5			1	
		Repair				1.0		1,4	G
12	Cable, Power (AC) (V)1, (V)2, (V)3, (V)4 Only	Test			0.5				C,F
		Replace			0.1				
		Repair			1.0			1,7	E
13	Cable, Power (DC) (V)1X, (V)2X, (V)3X, (V)4X Only	Test			0.5				C,F
		Replace			0.1				
		Repair			1.0			1,7	E
14	Cable, I/O All Versions	Test			0.5			1,4	
		Replace			0.1				
		Repair			0.1			1,7	E

SECTION II. MAINTENANCE ALLOCATION CHART
FOR
PROCESSING SET AN/UYK-64(V) - Continued

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQPT	(6) REMARKS
			C	O	F	H	D		
15	Core Memory Module (2019) (V)2, (V)2X,(V)4, (V)4X Only	Test			0.5			3,5	
		Replace			0.1			1,6	H
		Test					0.6	Depot Facilities	
		Repair					1.0	Depot Facilities	
16	Core Memory Controller (1755) (V)2, (V)2X, (V)4, (V)4X Only	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		2	G
17	Serial Aircraft Data Bus (3761)	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
18	Drive Adapter (4055)	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
19	Reporting Data Link Subsystem (TBD) (Host)	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G
20	Reporting Data Link Subsystem (TBD) (Receiver)	Test			0.5			3,5	
		Replace			0.1			1,6	
		Test				1.0		9	G
		Repair				1.0		1	G

SECTION III. TOOL AND TEST EQUIPMENT REQUIREMENTS FOR PROCESSING SET AN/UYK-64(V)

TOOL OR TEST EQUIPMENT REF CODE	MAINTENANCE CATEGORY	NOMENCLATURE	NATIONAL NATO STOCK NUM8ER	TOOL NUMBER
1	O,F,H,D	Tool Kit, Electronic Equipment TK-101/G	5180-00-064-5178	
2	F,H, D	Tool Kit, Electronic Equipment TK-105/G	5181-00-610-8177	
3	F	Test Set Group OQ-329/U	TBD*	
4	F,H	Multimeter AN/USM-451	6625-01-060-6804	
5	F	Diagnostic Tape	TBD*	
6	F,H,D	Card Extractor Tool	Model 5625 16-106458** FSCM 14345	
7	F,H,D	Connector Tool Kit	5120-00-146-6558	
8	F,H,D	Extender Card	Model 5621 100048-01** FSCM 14345	
9	H,D H	Maintenance Facilities W/AN/MSM-105 OQ-290 (V) l/MSM	6525-01-095-9312	

*NSN to be assigned by US Army
**Model/part numbers are ROLM Corporation FSCM 14345

SECTION IV. REMARKS
FOR
PROCESSING SET AN/UYK-64(V)

REFERENCE CODE	REMARKS
A	System level diagnostics and BITE utilized
B	Maintenance diagnostics will be utilized to detect and isolate to a defective PCB(s) with OQ-3Z9/u
C	Simple continuity tests on connectors and backplane wiring
D	Simple connector and wiring repairs
E	Organizational level replacement accomplished with spares obtained from D. S., based on system level diagnostic testing and system requirements
F	Continuity test
G	Special Repair Activity (SRA)
H	Memory set consists of inhibit, address and core stack and must be replaced as a set
I	Check output of power supply under load
J	Use end to end diagnostic routine
K	Throwaway item
L	Model 5711 Central Processor Unit consists of: Data Board, PROM (66) Board, PFP Board and MAP Board
M	Model 5710 Central Processor Unit consists of: Data Board, PROM (E) Board, PFP Board and MAP Board
N	Model 1751 Floating Point Unit consists of: FPU “A”’ Board, FPU “B” Board and FPU “C” (66) Board or FPU “A” Board, FPU “B” Board and FPU “C” (E) Board

APPENDIX D

ADDITIONAL AUTHORIZATION LIST FOR PROCESSOR AN /UYK-64(V) AND I/O INTERFACE

Section 1. INTRODUCTION

D-1. SCOPE

This appendix lists additional items you are authorized for the support of the processor and I/O chassis.

D-2. GENERAL

This list identifies items that do not have to accompany the processor and 1/0 chassis and that do not have to be turned in with it. These items are all authorized to you by CTA, MTOE, TDA, or JTA.

D-3. EXPLANATION OF LISTING

National stock numbers, descriptions, and quantities are provided to help you identify and request the additional items you require to support this equipment. The items are listed in alphabetical sequence by item name under the type document (i.e., CTA, MTOE, TDA, or JTA) which authorizes the item(s) to you.

SECTION II. ADDITIONAL AUTHORIZATION LIST

(1) NATIONAL STOCK NUMBER	(2) DESCRIPTION PART NUMBER AND FSCM USABLE ON CODE	(3) UNIT OF MEAS	(4) QTY AUTH
	MTOE AUTHORIZED ITEMS		
	INTERFACE UNIT MX-107374/UYK 80058 P/N 109713-01	EA	AR
5995-01-159-3620	INTERFACE UNIT MX107375/UYK 80058 P/N 109713-02	EA	AR
1440-01-148-0777	CCA, PRIORITY LOAD MODULE PL-1474/UYK 80058 P/N 106280-01	EA	AR
1440-01-149-3199	CCA, I/0 BUS EXPANDER PL-1467/UYK 80058 P/N 106680-01	EA	AR
	CCA, PAPER TAPE READER INTERFACE PL-1475/UYK 80058 P/N 100044-01	EA	AR
	CCA, LINE PRINTER INTERFACE PL-1473/UYK 80058 P/N 100691-01	EA	AR
	CCA, MAGNETIC TAPE CONTROLLER PL-1477/UYK 80058 P/N 106860-01	EA	AR
5999-01-160-0002	CCA, FLOPPY DISK INTERFACE PL- 1468/UYK 80058 P/N 106029-01	EA	AR
1440-01-148-0750	CCA, PROGRAMMABLE INTERVAL TIMER PL-1465/UYK 80058 P/N 106666-01	EA	AR
5999-01 -160-0007	CCA, PARALLEL I/0 BUFFER PL-1471 /UYK 80058 P/N 100298-01	EA	AR
1440-01-148-2142	CCA, DIFFERENTIAL 1/0 BUFFER, PL-1478/UYK 80058 P/N 100928-01	EA	AR
	CCA, SERIAL DIFFERENTIAL 1/0 INTERFACE PL-1480/UYK 80058 P/N 100730-01	EA	AR
5999-01-159-9999	CCA, SYSTEM INTERUPTS PL-1479/UYK 80058 P/N 100379-01	EA	AR
5999-01-159-9998	CCA, DATA CHANNEL CONTROLLER CONV PL-1470/UYK 80058 P/N 100284-01	EA	AR

SECTION II. ADDITIONAL AUTHORIZATION LIST

(1) NATIONAL STOCK NUMBER	(2) DESCRiPTION PART NUMBER AND FSCM USABLE ON CODE	(3) UNIT OF MEAS	(4) QTY AUTH
	MTOE AUTHORIZED ITEMS (Continued)		
5999-01-160-0008	CCA, ASYNCHRONOUS INTERFACE PL-1476/UYK 80058 P/N 100758-01	EA	AR
59901-160-0000	CCA, ASYNCHRONOUS MULTIPLEXER PL-1472/UYK 80058 P/N 100980-02	EA	AR
1440-01-148-0751	CCA, I/0 TESTER MODULE PL-1469/UYK 80058 P/N 100791-01	EA	AR
	CCA, KW-7 INTERFACE PL-1491 /UYK 80058 P/N 110615-11	EA	AR
7010-01-128-1817	CCA, RCU MULTIPLEXER PL-1482/UYK 80058 P/N 110444-01	EA	AR
5999-01-127-5869	CCA, CURRENT DRIVER PL-1483/UYK 80058 P/N 112119-01	EA	AR
	CCA, BEARING DESIGNATOR HEADING IND PL- 1490/UYK 80058 P/N 112908-01	EA	AR
	CCA, TT-580 INTERFACE PL-1489/UYK 80058 P/N 112912-01	EA	AR
7025-01-187-9310	CCA, ASYNCHRONOUS LINE MULTIPLEXER 1466/UYK 80058 P/N 107275-01	EA	AR
5999-01-155-0174	CCA, FIXED DISK ADAPTER PL-1499/UYK 80058 P/N 110424-01	EA	AR
6625-00-832-2199	CCA, MIL-STD 1553B PL-XXXX/UYK 80058 P/N 112373-01	EA	AR

APPENDIX E

EXPENDABLE SUPPLIES AND MATERIALS LIST

E-1. SCOPE

This appendix lists expendable supplies and materials needed to operate and maintain Data Processing Set AN/UYK-64 (V). These items are authorized by CTA 50-970, Expendable Items (Except Medical, Class V, Repair Parts and Heraldic [terns).

E-2. EXPLANATION OF COLUMNS

a. Column (1) — Item Number. This number is assigned to the entry in the listing and is referenced in the narrative instructions to identify the material; e. g., "Use cleaning compound (item 5, appx D)."

b. Column (2) — Level. This column identifies the level of maintenance that requires the listed item.

C = Operator/Crew
O = Organizational

c. Column (3) — National Stock Number. This is the National Stock Number assigned to the item; use it to request or requisition the item.

d. Column (4) - Description. Indicates the Federal item name and, if required, a description to identify the item. The last line for each item indicates the Federal Supply Code for Manufacturer (FSCM) in parenthesis followed by the part number.

e. Column (5) — Unit of Measure (U/M). Indicates the measure used in performing the actual maintenance function. This measure is expressed by a two-character, alphabetical abbreviation (e. g., ea, in, pr). If the unit of measure differs from the unit of issue, requisition the lowest unit of issue that will satisfy the requirements.

E-3. SPECIAL INFORMATION

National Stock Numbers (NSN) that are missing from section II to follow have been applied for and will be added to this technical manual by future change/revision when they are entered in the Army Master Data File (AMDF). Until the NSN have been established and published, submit exception requisitions to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, New Jersey 07703-5007 for the part required to support the equipment.

SECTION II. EXPENDABLE SUPPLIES AND MATERIALS LIST

(1) ITEM NO.	(2) LEVEL	(3) NATIONAL STOCK NUMBER	(4) DESCRIPTION PART NO. AND FSCM	UNIT OF MEAS.
1	C,O	6810-00-753-4493	Alcohol: Isopropyl (81 349) MIL-A-10428, Grade A	OZ
2	C,O	7920-00-356-4694	Brush: Bristle (81348)	EA
3	C,O	8305-00-267-3015	Cloth: Cheesecloth: Cotton: Lint-less (81 348) CCC-C-440, Type II, Class 2.	YD
4	C,O		Detergent: Mild: Liquid (TBD)	OZ
5	o		Dessicant Bags	EA
6	o		Plastic Bags (Chassis Size)	EA
7	o		Tape: Adhesive	EA
8	o		Container: Foam: Chassis Size	EA
9	o		Tape: Adhesive: Waterproof	FT
10	o		Cover: Foam: Chassis Size	EA
11	C,O		Material: Barrier	FT
12	o		Box: Fiberboard: Chassis Size	EA
13	o		Bag: Plastic: Forms and Tags	EA
14	o		Label: Shipping	EA

GLOSSARY

ALU	Arithmetic Logic Unit
AMDF	Army Master Data File
apex	Appendix
AIR	Air-Transport Rack
BITE	Built-In Test
CPU	Central Processing Unit
DISREP	Discrepancy in Shipment Report
DMA	Direct Memory Access
EIR	Equipment improvement Recommendations
ERCC	Error Correction Code
ESML	Expendable Supplies & Materials List
ETM	Elapsed Time Meter
FPU	Floating Point Unit
lMC/RMC	Internal Memory Control/Remote Memory Control
1/0	Input/Output
MAC	Maintenance Allocation Chart
MEMIN	Memory In
MEMOUT	Memory Out
MTU	Magnetic Tape Unit
NSN	National Stock Numbers
PCB	Printed-Circuit Boards
PFP	Prefetch Processor

GLOSSARY — Continued

PMCS	Preventive Maintenance Checks and Services
PROM	Programmable Read Only Memory
PWR	Power
RAM	Random Access Memory
ROD	Report of Discrepancy
TAMMS	The Army Maintenance Management System
TMDE	Test, Measurement, and Diagnostic Equipment
UART	Universal Asynchronous Receiver/Transmitter
VC	Virtual Console

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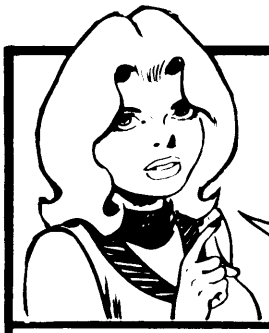
RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS



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10 July 1975

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TM 11-5840-340-12	23 Jan 74	Radar Set AN/PRC-76

BE EXACT PIN-POINT WHERE IT IS

PAGE NO	PARA-GRAPH	FIGURE NO	TABLE NO
2-25	2-28		
3-10	3-3		3-1
5-6	5-8		
		F03	

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

Recommend that the installation antenna alignment procedure be changed throughout to specify a 2^{o} IFF antenna lag rather than 1^{o}.

REASON: Experience has shown that with only a 1^{o} lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2^{o} without degradation of operation.

Item 5, Function column. Change "2 db" to "3db."

REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.

Add new step f.1 to read, "Replace cover plate removed in step e.1, above."

REASON: To replace the cover plate.

Zone C 3. On J1-2, change "+24 VDC to "+5 VDC."

REASON: This is the output line of the 5 VDC power supply. +24 VDC is the input voltage.

PRINTED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER
SSG I. M. DeSpiritof 999-1776

SIGN HERE
I. M. DeSpiritof

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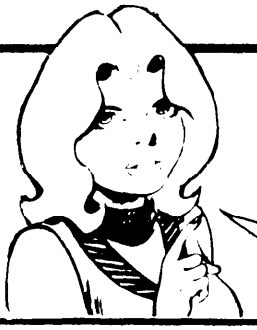

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TM 11-7021-202-12	5 Sep 85	Data Processing Sets AN/UYK-64(V)1 etc.

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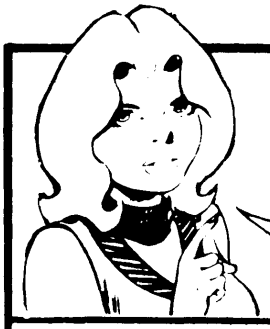

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