pdp 8/s

serial # 201

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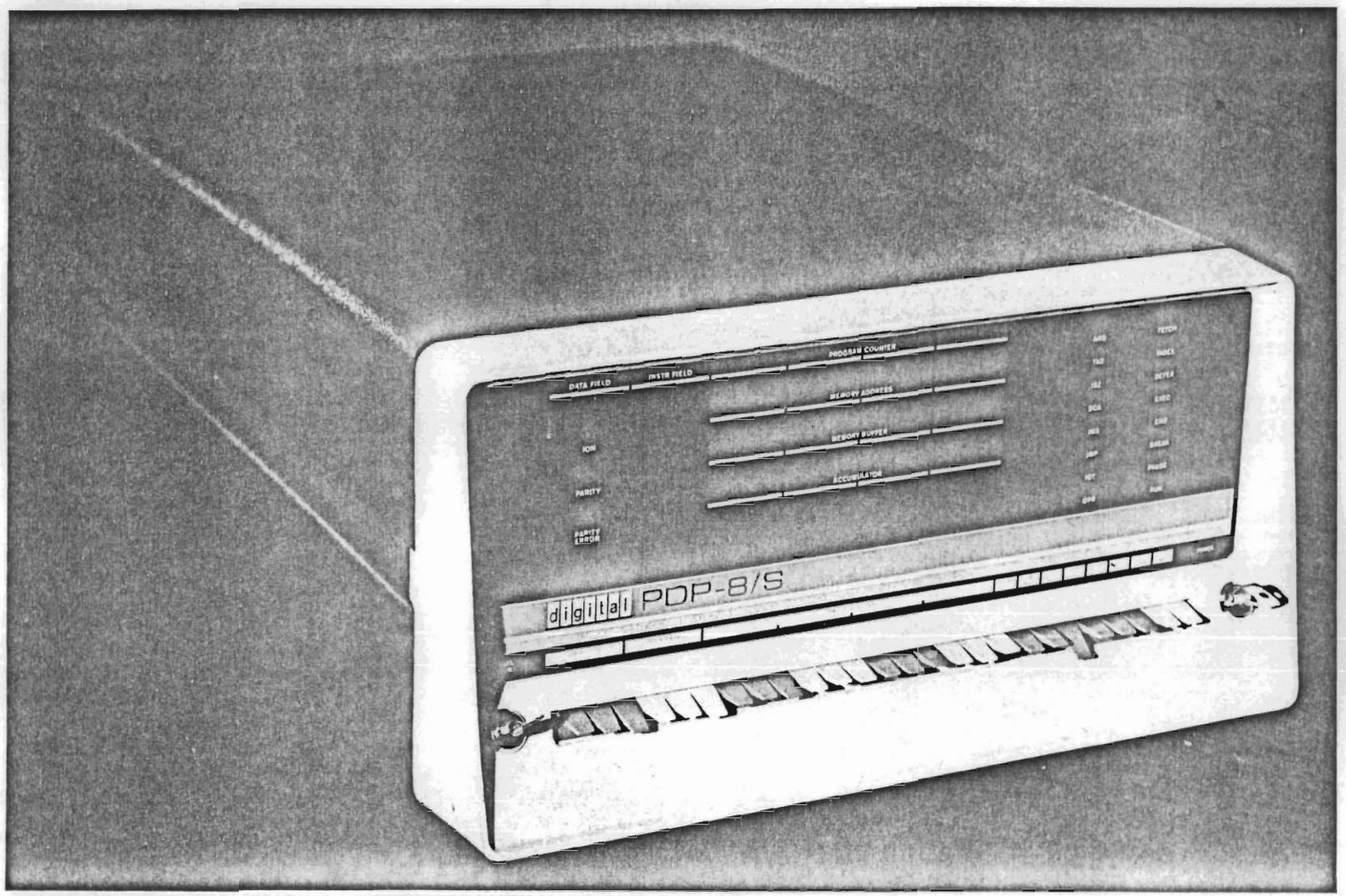


Programmed Data Processor-8/S

PREFACE

This instruction manual is intended to aid personnel in the operation and maintenance of the PDP-8/S. The manual also discusses the operation of the Teletype ASR 33 and describes its control unit, which is of DEC manufacture, but a separate manual is furnished for the device itself.

The first two chapters present a general description of the system and its operation. Chapter 1 lists the operating specifications of the system and describes its physical and electrical characteristics. Chapter 2 describes the logical organization of the computer, discusses the number system and instruction formats used by it, explains the use of all controls and indicators on the operator panel, and explains the operation of the ASR 33.

Chapter 3 presents a complete, detailed description of the system logic, including a discussion of the symbols and notation used in the logic drawings and flow charts. Chapter 4 contains information useful in maintaining the system, including a discussion of maintenance programs, memory alignment and troubleshooting procedures, and in-out bus specifications.

Following Chapter 4 is Appendix A which contains engineering drawings, logic drawings, flow charts and circuit schematics.

CHAPTER 1
INTRODUCTION

The PDP-8/S is a small-scale, general-purpose digital computer designed for use as an independent information-handling facility in a larger computer system, or as the control element in a complex processing system. The basic computer consists of a central processor and a memory, and has a Teletype Model 33 Automatic Send/Receive set for input-output. The processor performs all arithmetic, logical and system control functions. Memory operation is based on a read-write cycle, one cycle being executed each time access is requested by the processor.

Interface circuits for the in-out bus allows connection to a variety of peripheral equipment. Every device must detect its own selection code and provide any necessary input gating. In the standard computer all transfers over the in-out bus are under program control, but peripheral equipment can interrupt the program. Optional equipment allows direct data access to the memory for high speed devices such as disc memory.

In the processor all operations on words are serial; the computer uses parallel transfers only for communication between the processor and the memory, the console, or the in-out equipment over the in-out bus. Information handled by processor and memory has the following characteristics.

Word Length	
Processor:	12 bits
Memory:	13 bits including parity bit
Instruction Format	
Memory Reference:	Instruction code, 3 bits Indirect, 1 bit Memory address, 8 bits
Operate Group:	Instruction code, 12 bits
Input-Output:	Instruction code, 12 bits including 6 bit device code
Internal Number System	Binary
Negative Representation	Two's complement
Number Format	Sign, 1 bit; magnitude, 11 bits

All timing is synchronous, but processor and memory operate on separate clocks, which cannot run simultaneously. Thus every time that the processor requests memory access its clock stops; when the memory cycle is complete, the processor restarts. Each processor cycle of 10.5 μs is one word time, the time required to process one word serially. The PDP-8/S uses two types of random access magnetic

core memory having cycle times of 6.3 and 6.5 μs. Instruction execution times differ depending upon the number of processor and memory cycle required, and upon whether a given instruction uses indirect addressing and autoindexing.

The processor must set up all transfers of data to and from the peripheral equipment; but since a device can signal the processor by means of a program interrupt when it requires services, no processor time need be lost in waiting, and processor and peripheral equipment can operate in parallel. The only I/O device supplied with the standard computer is the Teletype Model 33 ASR but it includes keyboard, printer, tape reader and punch. It handles data at the rate of ten 8-bit characters per second.

1.1 PHYSICAL CHARACTERISTICS

The table model is housed in a cabinet but the computer is also available for mounting in a standard 19-in. rack. The computer contains six logic mounting panels, lettered A to F from right to left when viewing it from the front. Each mounting panel can hold forty DEC Flip-Chip plug-in modules numbered from front to back.

The rack-mountable model requires 10-1/2 in. of vertical space in a 19-in. rack. It protrudes 3-3/4 in. at the front of the rack, and slides out 25 in. Physical dimensions of both models are shown in Figures 1-1 through 1-5. The table model weighs 84 lb, and the rack model weighs 200 lb including power equipment. The Teletype ASR 33 has the following dimensions.

Height: 45 in.
Width: 22 in.
Depth: 19 in.
Weight: 100 lb

Intake fans at the back of the table model cool the logic modules by blowing air between them. A PDP-8/S shipped mounted in a DEC rack has three muffin fans on the left side, but the user must supply adequate ventilation for a computer shipped unmounted.

It is recommended that the ambient temperature at the installation be maintained between 70° and 85°F, but it can vary between 32° and 130°F without adverse effect. Although all exposed surfaces are treated to prevent corrosion, exposure to extreme humidity for long periods of time should be avoided.

1.2 ELECTRICAL CHARACTERISTICS

The computer uses standard line power at 115 ± 17 Vac, 60 cycle (±2%), single phase. The rack model uses a standard 728 power supply and a control through which the power switch on the front panel switches ac to a pair of receptacles on the computer backplate. These receptacles are for the power supply and the fans. To switch ac to other supplies or devices from the computer front panel

requires the use of a repeater relay slaved to this switched ac. The power cable uses a Hubbell Twist-Lok connector; both cable and connector are rated at 20 or 30 amp depending upon total system requirements.

The table model has an equivalent power supply mounted on the inside rear of the cabinet, and both it and the fans receive ac through the front panel power switch and a pair of circuit breakers. The power cable uses a standard ac plug with ground and is rated at 15 amp. The teletype must be powered separately.

Current consumption is as follows.

	Processor	Teletype
Line current	3 amp	2.6 amp Turn on surge, 7 amp
Dissipation	100W	140W
Logic voltages		
+10V	0.6 amp	1.2 amp
-15V	5.5 amp	0.5 amp

The dc voltages required by the logic are +10V and -15V. All logic is solid state; transistors and diodes operate on static logic levels of 0 and -3Vdc (tolerances are 0V to -0.3V and -3.2V to -3.9V). Most logic modules include an internal supply to derive the negative logic level from the -15V input. PDP-8/S logic uses pulse timing almost exclusively. Pulse amplitude from a pulse generating source is +3V from -3V with the same tolerances as levels. Pulses at inverter outputs may be from ground to -3V or vice versa. Pulse widths may be 100 ns or 400 ns depending upon application. Occasionally, an input may be triggered by a positive level transion of 60 ns or less instead of a pulse. Driving voltages for the core memory are nominally -10V to ground and -15V to ground. The statistics given here apply to all modules used in the equipment described in this manual except the transmitter and receiver modules for the teletype; the special voltage requirements for these modules are discussed with the teletype logic.

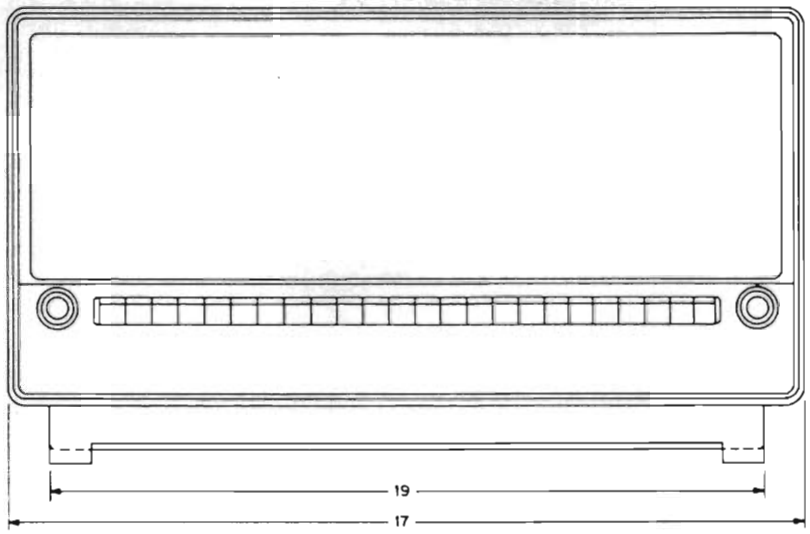


Figure 1-1 Dimensions, Table Model (Front View)

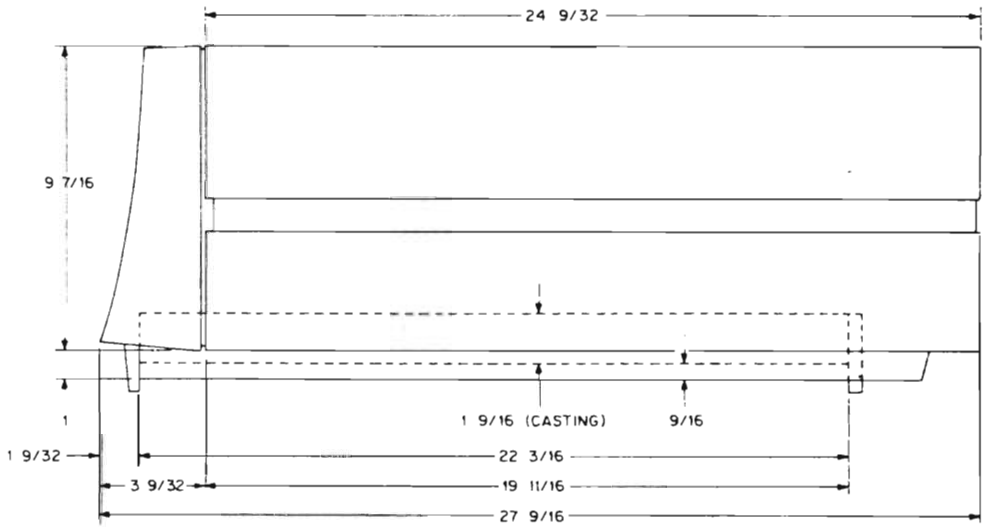


Figure 1-2 Dimensions, Table Model (Side View)

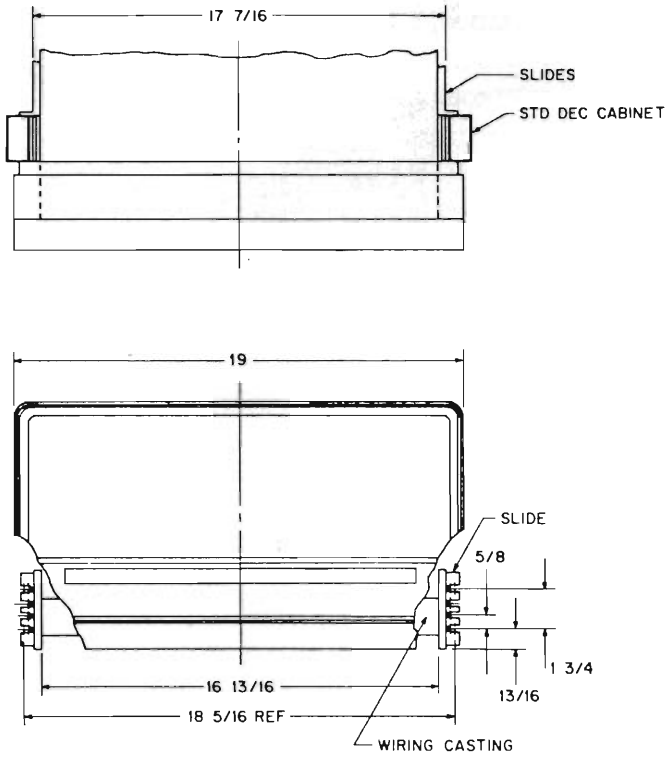


Figure 1-3 Dimensions, PDP-8/S Mounted in Standard DEC Rack

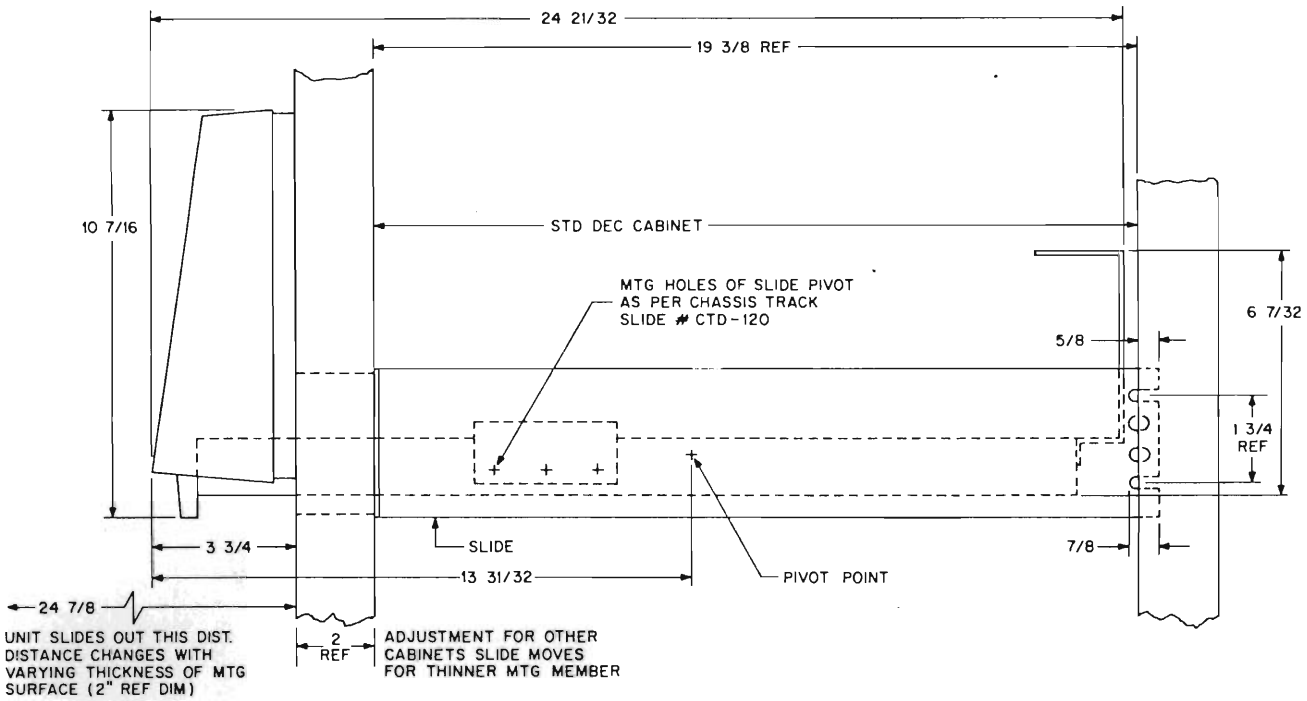


Figure 1-4 Dimensions, PDP-8/S Mounted in Standard DEC Rack

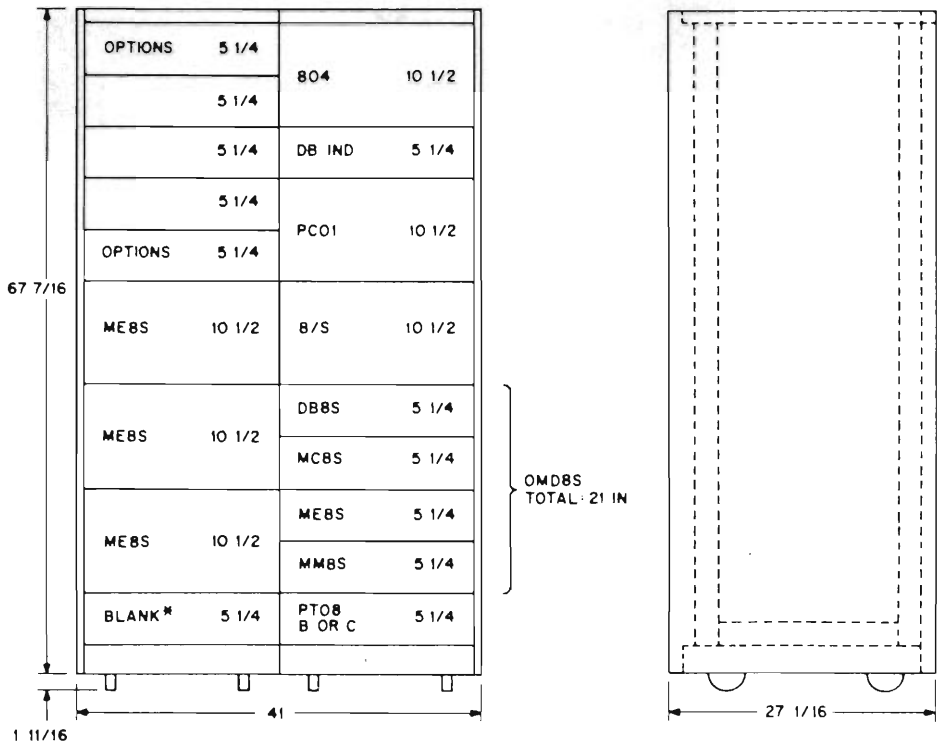


Figure 1-5 Typical Rack Mounted PDP-8/S
with Recommended Option Mounting

CHAPTER 2
SYSTEM OPERATION

Figure 2-1 shows the registers and data flow in the PDP-8/S. The processor is the control unit for the entire system: it governs all peripheral in-out equipment, sequences the program, and performs all arithmetic and logical operations.

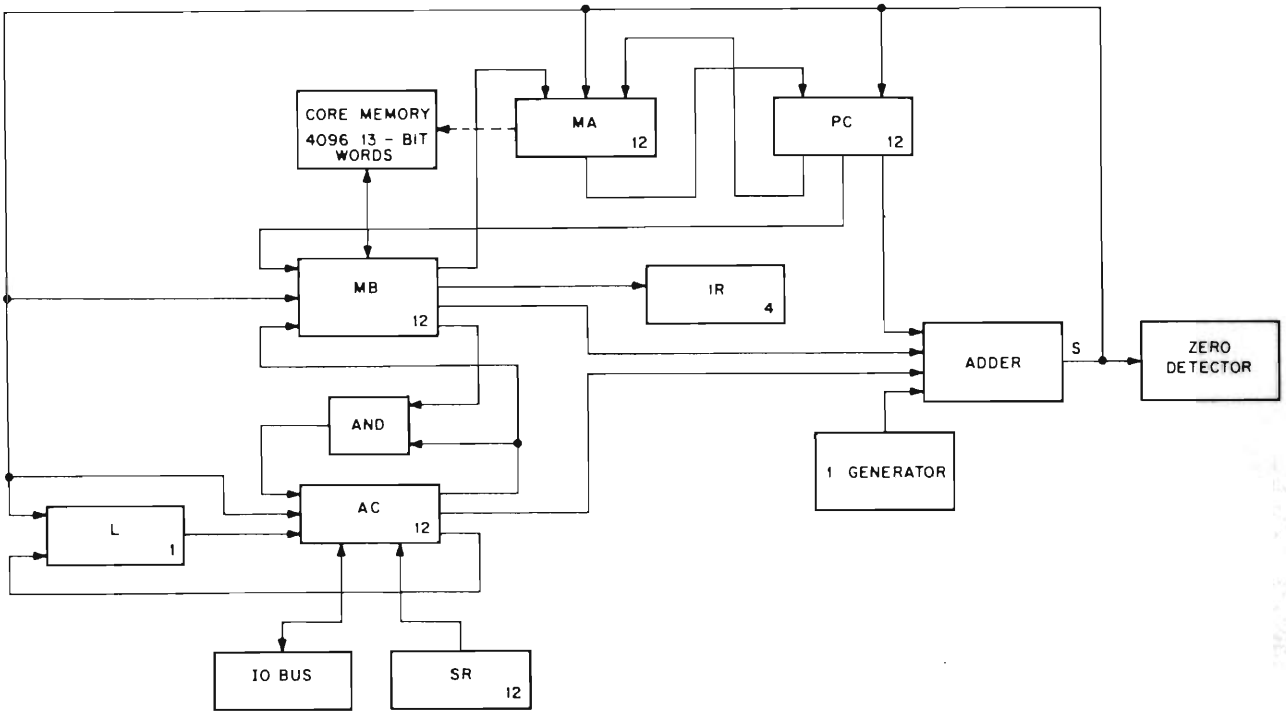


Figure 2-1 PDP-8/S Data Flow

The processor handles words of 12 bits, which are stored in a memory with a capacity of 4096 words. Storage in memory is actually in the form of 13-bit words, the extra bit being an even parity bit for the word. The bits of a word are numbered 0 through 11, left to right, as are the flip-flops in the registers that handle the words. Words are used either as computer instruction in the program, as addresses, or as operands, that is, data for the program.

The processor performs a program by executing instructions retrieved from consecutive memory locations, as counted by the program counter (PC), although the program may alter its own sequence by changing the address in PC, either by indexing (incrementing it by one) an extra time in a test skip instruction or by replacing its contents with the value specified by a jump instruction. To gain access to memory for retrieval or storage, the processor requests a memory cycle and supplies an address from the memory address register (MA). All transfers of data between processor and memory are made through the memory buffer (MB). When a word is retrieved at MB, as an instruction, its left four bits pass to the instruction register (IR), which is decoded to govern the actual execution of the instruction. In a memory reference instruction, the rest of the word in MB supplies address information to MA; otherwise the rest of the word is decoded directly from MB to assist in instruction execution.

The heart of the processor is the memory buffer MB, the accumulator (AC), and a 1-bit serial adder. All transfers between processor and peripheral equipment are made via AC, which is connected to the in-out bus. The accumulator is also connected to the switch register (SR) through which the operator can send data and addresses into the computer from the console. The only parallel transfers that occur in the system are those between MB and memory, between AC and the I/O bus, and from SR to AC. All other operations in the processor are serial: all registers are shift registers, and information is transferred from one register to another by shifting both registers to the right, so that information leaves one register at the right (LSB) and enters the other from the left (MSB). Although not shown in Figure 2-1, the processor can recirculate any of the four main registers whenever its contents must be saved while being transferred.

To produce the logical AND function, the contents of MB and AC are shifted through a simple AND gate, with the result appearing in AC. All other operations on words are performed through the serial adder. The contents of MB and AC are added one bit at a time as the sum is shifted into AC. The adder is also used to increment AC, MB, or PC, to complement AC, and even to detect zero contents in MB or AC for a skip test.

Associated with AC is a 1-bit register, the link (L). The link serves as an overflow flag in addition and when AC is incremented. AC and L can be rotated together, to the left or right, as a single 13-bit register (left rotation is produced by a shortened right shift). The program can also use L to generate products and quotients one bit at a time.

Besides the registers that enter into the regular execution of the program and its instructions, the processor also contains a program interrupt system that allows peripheral devices, a memory parity error or a power failure to interrupt normal program flow. When such an interruption occurs and the interrupt is on (ION), the processor stores the current contents of PC (the address of the next instruction in the program) in location 0000, and executes the instruction in location 0001.

Timing for all operations in processor and memory is supplied by two clocks. Each serial processing of a word is performed in one word time under control of the processor clock. When memory access is required, the processor stops its own clock and triggers a memory cycle, which is executed under control of the memory clock. At the completion of the memory cycle the memory clock stops, and the processor clock restarts to execute another word time.

2.1 PROGRAMMING

The program is a set of instructions used to perform some task and is stored in memory. Each word in memory is identified by an address, 0000-7777 octal. To execute a program, the computer normally retrieves instructions from sequentially increasing locations, but the instructions, themselves, can alter program flow and cause the computer to continue sequential operation from some other location. Table 2-1 is an instruction index.

Table 2-1.
Instruction Index

Mnemonic	Meaning	Octal Code
AND	Logical AND	0xxx
TAD	Twos Add	1xxx
ISZ	Increment and Skip if Zero	2xxx
DCA	Deposit and Clear Accumulator	3xxx
JMS	Jump to Subroutine	4xxx
JMP	Jump	5xxx
IOT	In-out Transfer	6xxx
OPR	Operate	7xxx
	Operate Group	
NOP	No Operation	7000
IAC	Increment Accumulator	7001
RAL	Rotate Accumulator Left	7004
RTL	Rotate Two Left	7006
RAR	Rotate Accumulator Right	7010
RTR	Rotate Two Right	7012
CML	Complement Link	7020
CMA	Complement Accumulator	7040
CIA	Complement and Increment Accumulator	7041
CLL	Clear Link	7100
STL	Set Link	7120
CLA	Clear Accumulator	7200
STA	Set Accumulator	7240
HLT	Halt	7402
OSR	OR Switch Register	7404
SKP	Skip	7410
SNL	Skip on Nonzero Link	7420
SZL	Skip on Zero Link	7430
SZA	Skip on Zero Accumulator	7440
SNA	Skip on Nonzero Accumulator	7450
SMA	Skip on Minus Accumulator	7500
SPA	Skip on Positive Accumulator	7510

Table 2-1. (continued)
Instruction Index

Mnemonic	Meaning	Octal Code
CLA	Clear Accumulator	7600
LAS	Load AC Switches	7604
	IOT Group	
ION	Interrupt On	6001
IOF	Interrupt Off	6002
SMP	Skip on No Memory Parity Error	6101
CMP	Clear Memory Parity Error Flag	6104
KSF	Keyboard, Skip on Flag	6031
KCC	Keyboard, Clear Flag	6032
KRS	Keyboard, Read Buffer Static	6034
KRB	Keyboard, Read Buffer	6036
TSF	Teleprinter, Skip on Flag	6041
TCF	Teleprinter, Clear Flag	6042
TPC	Teleprinter, Print Character	6044
TLS	Teleprinter, Load Sequence	6046

2.1.1 Number System

The PDP-8/S uses two's complement, fixed-point conventions to do binary arithmetic. In a word used as a number, bit 0 (the left-most bit) represents the sign denoted by 0 for positive, 1 for negative. In a positive number, the remaining eleven bits are the magnitude in ordinary binary notation. The negative of a number is obtained by taking the two's complement. If x is an n-digit binary number, its two's complement is $2^n - x$, and its one's complement is $(2^n - 1) - x$, or equivalently $(2^n - x) - 1$. Subtracting a number from $2^n - 1$ (from all 1s) is equivalent to performing the logical complement, changing all zeros to ones and all ones to zeros. Therefore, to form the two's complement, take the logical complement (usually referred to merely as the complement) of the entire word including the sign, and add 1 to the result. In a negative number, the sign bit is 1 and the remaining bits are the two's complement of the magnitude.

$+153_{10} = +231_8 =$ 000 010 011 001
(bit 0 … bit 11)

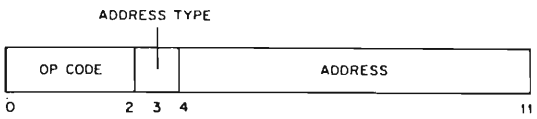
$-153_{10} = -231_8 =$ 111 101 100 111
(bit 0 … bit 11)

Zero is represented by a word containing all 0s; complementing this number produces all 1s, and adding 1 to that produces all 0s again. There is only one zero representation and its sign is positive. Since the numbers are symmetrical in magnitude about a single zero representation, all even numbers both positive and negative end in 0, all odd numbers in 1 (a number all 1s represents -1). Since there are the same number of positive and negative numbers, however, there is one more negative number than there are nonzero positive numbers. This is the most negative number and it cannot be produced by negating any positive number. (The magnitude of the most negative number is one greater than the largest positive number.)

If one's complements were used for negatives, a negative number could be read by attaching significance to the 0s instead of the 1s. In two's complement notation, each number is one greater than the complement of the positive number of the same magnitude, so one can read a negative number by attaching significance to the rightmost 1 and attaching significance to the 0s at the left of it. (The negative number of largest magnitude has a 1 in only the sign position.) In a negative integer, 1s may be discarded at the left, just as leading 0s may be dropped in a positive integer. In a negative fraction, 0s may be discarded at the right as long as only 0s are discarded, the number remains in two's complement form because it still has a 1 that possesses significance. If a portion including the rightmost 1 is discarded, the remaining part of the fraction is now a one's complement. The computer does not keep track of a binary point, so the programmer must adopt a point convention and shift the magnitude of the result to conform to the convention used.

2.1.2 Instruction Format

A computer instruction performs some basic function, such as storing a word in memory or performing an arithmetic or logical operation. If an instruction requires a memory address, the three high-order bits (0 through 2) specify the operation, bit 3 specifies the type of addressing, and the remaining eight bits (4 through 11) specify the effective address or the location to be used in determining the effective address. The effective address is the actual address used to fetch the operand or alter program flow.



The operate and in-out instructions do not require memory addresses. In an operate instruction bits 0 through 2 contain 7, and the remaining bits specify individual operations, so an instruction can be microprogrammed to perform a combination of the various operations. In an in-out instruction,

bits 0 through 2 contain 6, bits 3 through 8 specify the in-out device, and bits 9 through 11 select the timing pulses sent out over the I/O bus. Pulses at the three event times, in order, are selected respectively by 1s in bits 11, 10, and 9.

2.1.3 Addressing

Locations in memory are addressed by the 12-bit octal numbers 0000 to 7777 (0 to 4095 decimal). The instruction format allows only eight bits for an address, so for programming purposes the memory is divided into thirty-two pages, each containing 128 (200_8) locations. The eight address bits in the instruction can select one location out of 256, or a single location from two pages. If bit 4 is 0, bits 5 through 11 are taken as an address in page 0, i.e., the address part of the instruction is taken to represent an address between 0000 and 0177. If bit 4 is 1, bits 5 through 11 are taken as an address in the same page from which the instruction was retrieved. The 12-bit address that is used is the combination of bits 5 through 11 of the instruction word and bits 0 through 4 of the address previously supplied by PC to MA for instruction retrieval.

Bit 3 of the instruction word specifies the type of address contained in bits 4 through 11. If bit 3 is 0, addressing is direct; the effective address is the 12-bit address determined by bits 4 through 11. If bit 3 is 1, addressing is indirect, and the address part of the instruction is taken to specify a location whose contents are to be used as the (12-bit) effective address.

2.1.4 Autoindexing

The program can make use of an automatic indexing feature by indirectly addressing any memory location from 0010 to 0017. Whenever one of these locations is specified by an indirect address, the processor retrieves the contents of the addressed location, indexes the word contained therein, writes the altered word back into memory, and uses the indexed word as the effective address.

2.1.5 Operating Speed

The table 2-2 gives the approximate execution times in microseconds of the various PDP-8/S instructions. Where they are applicable, the longer times that are required for indirect addressing and autoindexing are also given. With each time, the pair of numbers separated by a comma indicates the number of processor and memory cycles required for the instruction.

Table 2-2.
PDP-8/S Instruction Execution Times

			Indirect Addressing		Autoindexing	
AND	32.2	2,2	48.3	3,3	64.4	4,4
TAD	32.2	2,2	48.3	3,3	64.4	4,4
ISZ	48.3	3,3	64.4	4,4	80.5	5,5
DCA	42.7	3,2	58.8	4,3	74.9	5,4
JMS	42.7	3,2	58.8	4,3	74.9	5,4
JMP	26.6	2,1	42.7	3,2	58.8	4,3
IOT	37.1	3,1				
OPR 1	26.6	2,1				
OPR 2	37.1	3,1				

A processor cycle (one word time) requires 10.5 μs if there is no memory request, about 9.8 μs otherwise. The above times are based on a memory cycle of 6.3 μs. The nominal times for the two memory types are 6.3 μs and 6.5 μs, but either type can differ by as much as 100 ns from its nominal value. Moreover, if the optional data channel equipment or expanded memory is added to the computer, the memory cycle time is fixed at 8 μs regardless of stack type. The programmer is advised not to use internal computer timing in place of a real-time clock.

A program interrupt takes 32.2 μs (2,2) in addition to instruction execution time. The first IOT pulse occurs 10.5 μs after the IOT instruction is fetched, and the other two pulses occur at 1-μs intervals thereafter.

2.2 Word Times

Each word time is made up of 14-bit times (numbered 00 through 13) during which the clock generates a string of fourteen bit pulses 750 ns apart. The first 12 pulses perform whatever serial operations are required on one or more 12-bit words. The thirteenth pulse performs most of the individual operations that are required for any instruction (such as an OPR), checks parity, and requests a memory cycle if one is required. When a memory cycle is requested, the processor clock stops, and the memory goes through its cycle controlled by its own clock. Upon completion of the cycle, the processor clock restarts at the fourteenth pulse, which determines the transition to the next word-time. When the computer is stopped by the program or the operator, it does so between the thirteenth and fourteenth bit times, i.e., at time 13 but following completion of the memory cycle if one is requested.

The word-time in which a word is processed depends upon what type of information it represents (an instruction, an address, an operand) and what functions must be performed on it. There are six word-times: fetch, index, defer, execute, end, break. Although the execution of an instruction

begins in fetch time, the program must start in end time, which determines the location of the first instruction and requests a memory cycle to retrieve it. In other words, fetch time does not fetch the instruction. Fetch time processes the instruction just retrieved from memory. It transfers the instruction code to IR for decoding, transfers the address part to MA, and indexes PC so that it will point to the next location.

At the end of fetch time, the processor requests memory access if the instruction is indirectly addressed or requires the retrieval of an operand. If an autoindexing location is indirectly addressed, the processor then enters index time; for any other indirect addressing it enters defer time; in any other situation it goes directly to execute time. In index time the address that has been retrieved is incremented by one and written back in memory. The processor then enters defer time to move the new address to MA and request a memory cycle, if an operand must be retrieved. The actual logical, arithmetic or program control operation specified by the instruction is then performed in execute time, which requests access if an operand must be deposited in memory. In end time the processor determines the location of the next instruction and fetches it. In some cases the execute and end times are simultaneous; if they are not, the processor automatically goes from execute to end time.

After retrieving an instruction, the processor returns to fetch time unless a program interrupt has been requested. In this case the processor enters break time in which it deposits the current contents of PC in location 0000, and then returns to end time to retrieve the instruction in location 0001. There are also three special word times for operations associated with the console: these are used for loading a starting address into PC, depositing a word in memory, or examining the contents of a memory location.

To control the special operations required for in-out, including parallel transfer over the bus, the first bit pulse in execute time of an IOT triggers a string of three special pulses 1 μs apart. Of these, the only pulses actually sent over the bus for use in IOT operations are those specified by the programmer in bits 9 through 11 of the IOT instruction.

2.3 PROCESSOR OPERATION

In the table model of the PDP-8/S, the circuit breakers are mounted on the rear panel with the power supply; the rack mounted model has a power control that includes circuit breakers and usually a power light. All other controls and indicators for the processor and memory are located on the computer front panel. The indicators are on the vertical upper part of the panel; below this is a row of two-position keys and switches with a key-operated rotary switch at each end (switches are alternate action, keys are momentary contact).

The six switches at the left end of the row and the corresponding lights at the top of the panel are for the optional memory expansion. The next 12 switches make up a switch register through which the operator can supply data and addresses to the processor (the up position of a switch represents a 1).

The register can be used in conjunction with some of the operating keys, and its contents can be read into AC by the program. The next six levers are the operating keys. They are off when in the up position, except for DEP (third one from the left) which is off when in the down position. The last two levers are the operating mode switches, which are off when in the down position. Power is applied to the computer by turning clockwise the key-operated POWER switch at the right-hand end of the panel. The similar PANEL LOCK switch at the left-hand end disables the operating keys and switches when turned clockwise (the last eight levers at the right-hand end become inoperative and the switch register is not affected).

When any indicator is lit, the associated flip-flop is in the 1 state or the associated function is true. A few indicators display useful information while the processor is running, but most change too frequently and are therefore discussed in terms of the information they display when the processor has stopped.

2.3.1 Indicators, Operating Keys, and Switches

In the center of the panel there are four rows of indicators that display (from top to bottom) the contents of PC, MA, MB and AC. The extra light at the left-hand end of the bottom row displays the contents of the link. When the computer stops, PC usually holds the address of the next instruction, MA indicates the address of the last memory access, and MB holds the word read from or written into memory.

Indicator	Function
FETCH, INDEX, DEFER, EXEC, END, BREAK	EXEC and END can be on together, but otherwise only one of these lights can be on at a time. The on light indicates the word time the processor has stopped in.
PAUSE	A memory cycle is in progress. This light can stay on long enough to be noticed only if optional data break equipment is occupying the memory most or all of the time, and thus the processor is running little if at all.
RUN	The processor is in normal operation with one instruction following another. When the light goes off, the computer stops.
AND, TAD, ISZ, DCA, JMS, JMP, IOT, OPR	Only one of these can be on at a time. It indicates the instruction being executed or just executed. If the processor stops with BREAK on, or the operator has just loaded an address from the console, the AND light will be on regardless of what instruction was last executed.
ION	The program interrupt system is on, so a parity error or an interrupt request over the in-out bus will cause a program break.
PARITY	Displays the parity bit of the last word read from or written into memory.
PARITY ERROR	Indicates that a word read from memory had incorrect parity.

When the computer executes a HLT, it stops with RUN and PAUSE off, and END and OPR on. The MB lights display the next instruction, the PC and MA lights indicate the address of the next instruction to be executed, i.e., the instruction just retrieved from memory in end time.

Operating Key	Function
START	Pressing this key clears AC, L, MB and the in-out equipment. It turns off ION, PARITY, and PARITY ERROR. It sets the END state, and lights RUN, causing the computer to begin normal operation by retrieving an instruction from the location currently addressed by PC.
LOAD ADD	If RUN is off, pressing this key clears AC. It turns off ION and loads the contents of the switch register into PC, and lights FETCH and AND.
DEP	If RUN is off, lifting this key deposits the contents of the switch register into the memory location currently addressed by PC, increments PC by one, and lights FETCH. At the completion of the operation, the AC and MB lights display the word deposited, PARITY indicates its parity, MA addresses the location into which the word was deposited, and PC contains the next consecutive address.
EXAM	If RUN is off, pressing this key turns off PARITY ERROR, clears AC, displays the contents of the memory location addressed by PC in the MB and PARITY lights. It increments PC by one, and lights FETCH. At the end of the operation MB and PARITY display the word, MA addresses the location that was examined, and PC addresses the next consecutive location.
CONT	Pressing this key lights RUN, causing the computer to begin normal operation in its current state. If RUN is already lit the key has no effect.
STOP	Pressing this key while RUN is lit causes the computer to stop with FETCH lit. At this time the instruction lights indicate which instruction is about to be executed, MB contains the instruction word or operand (or an address if an indirect bit was used) depending on the type of instruction, and PC points to the location one beyond that from which the instruction was retrieved. The MA lights indicate the address from which the last memory word was fetched. They represent either the address of the instruction or the operand (or an address if an indirect bit was used) depending on the type of instruction. The instruction indicators will display the type of instruction.

Operating Switch	Function
SING INST	While this switch is in the up position, the processor stops in fetch time of every instruction that it executes. Hence the operator can run a program one instruction at a time, by turning on this switch, fetching the first instruction by pressing START, and executing each succeeding instruction by pressing CONT. Each time the computer stops, the lights display the same information as when the STOP key is pressed.
SING STEP	While this switch is in the up position, the processor stops at the end of every word-time that it executes. This switch is for maintenance purposes and allows the operator to run a diagnostic routine or other program, one

SING STEP (continued)

step at a time. Operations are begun by pressing START, and each succeeding word-time is initiated by pressing CONT. The reader can determine the information that should be displayed on the panel by consulting the flow charts.

2.4 TELETYPE OPERATION

The teletype provides two-way communication between operator and computer. It is actually four devices: keyboard, printer, reader and punch, which may be operated in various combinations. The equipment operates at speeds up to ten characters per second, with 8-bit characters plus start and stop control signals transmitted serially.

Figure 2-2 Teletype Model ASR 33

Located at the right front right-hand side of the unit is a 3-position rotary switch LINE/OFF/LOCAL. When this switch is set to LOCAL, the entire unit is independent of the computer and the keyboard and printer function together as a normal typewriter. Moreover, turning on the punch allows the operator to punch a tape from the keyboard, and running the reader allows a tape to control the printer (if the punch is also on, it duplicates the tape).

Turning the switch to LINE connects the unit to the computer and separates its input and output functions. Any information transmitted to the computer from the keyboard affects the printer only insofar as the computer sends it back. Turning on the reader places it under program control, and turning on the punch causes it to punch whatever is sent to the printer by the computer.

The only control on the reader is a 3-position switch. When the switch is in the FREE position, the tape can be moved by hand freely through the reader mechanism. The STOP position engages the reader clutch so the tape is stationary but the reader is still off. Turning the switch to START causes the reader to read the tape if the unit is in local, but places it under program control if on line.

The operator controls the punch by means of four pushbuttons. The two on the right turn the punch on and off. Pressing the REL button releases the tape so that it can be moved by hand through the punch mechanism. Pressing B. SP. moves the tape backward one frame so that the operator can delete a frame that is incorrect by using the RUB OUT key (rubout characters are ignored when the tape is read).

The keyboard resembles that of a standard typewriter with four rows of keys and a space bar. The line feed moves the carriage only vertically with a spacing of six lines per inch. The return moves the carriage to the left margin but does not feed a line. To start a new line, the operator must strike both return and line feed. Codes for the characters on the lower parts of the key tops can be transmitted merely by striking the keys. Codes for printable characters on the upper parts (punctuation, ampersand, percent sign) are transmitted by holding down the shift key when striking the character key. Control codes are transmitted by holding down the control key CTRL, while striking the appropriate character key. Codes for all characters listed on the keyboard and some that are not can be transmitted to the computer, but codes for some of the control functions have no effect on the printer when sent back. Table 2-3 lists all codes, their ASCII assignments, and the key combinations required to transmit them. The 8-bit codes are listed below. An asterisk indicates a code that nas no effect on the Model 33. The characters actually contain only seven information bits; the eighth bit may be used for parity, but currently all machines are set up so that the eighth bit is a mark, and thus the codes generated from the keyboard are 200_8 greater than the corresponding ASCII codes.

Table 2-3.
Teletype Code

Octal Code	ASCII Character	Key Combination	Remarks
200	NULL	SHIFT CTRL P	Null
201*	SOM	CTRL A	Start of message
202*	EOA	CTRL B	End of address
203*	EOM	CTRL C	End of message
204	EOT	CTRL EOT	End of transmission; shuts off TWX machines
205	WRU	CTRL WRU	"Who are you?" Triggers "Here is...," at remote station
206*	RU	CTRL RU	"Are you...?"

Table 2-3. (continued)
Teletype Code

Octal Code	ASCII Character	Key Combination	Remarks
207	BELL	CTRL BELL	Rings the bell
210*	FE	CTRL H	Format effector
211	HT	CTRL TAB	Horizontal tab
212	LF	LINE FEED	Line feed
213	VTAB	CTRL VT	Vertical tab
214	FF	CTRL FORM	Form feed
215	CR	RETURN	Carriage return
216*	SO	CTRL N	Shift out
217*	SI	CTRL O	Shift in
220*	DC0	CTRL P	Device control reserved for data line escape
221	DC1	CTRL Q	Turns reader on
222*	DC2	CTRL TAPE	Turns punch on
223	DC3	CTRL XOFF	Turns reader off
224*	DC4	CTRL	Turns punch off
225*	ERR	CTRL U	Error
226*	SYNC	CTRL V	Synchronous idle
227*	LEM	CTRL W	Logical end of media
230*	S0	CTRL X	Separator, information
231*	S1	CTRL Y	Separator, data delimiter
232*	S2	CTRL Z	Separator, words
233*	S3	SHIFT CTRL K	Separator, groups
234*	S4	SHIFT CTRL L	Separator, records
235*	S5	SHIFT CTRL M	Separator, files
236*	S6	SHIFT CTRL N	Separator, miscellaneous
237*	S7	SHIFT CTRL O	Separator, miscellaneous
240	Space	Space bar	
241	!	SHIFT !	
242	"	SHIFT "	
243	#	SHIFT #	
244	$	SHIFT $	
245	%	SHIFT %	

Table 2-3. (continued)
Teletype Code

Octal Code	ASCII Character	Key Combination	Remarks
246	&	SHIFT &	
247	'	SHIFT '	
250	(	SHIFT (	
251	)	SHIFT)	
252	*	SHIFT *	
253	+	SHIFT +	
254	,	,	
255	-	-	
256	.	.	
257	/	/	
260	ø	0	Zero, prints with a slash
261	1	1	
262	2	2	
263	3	3	
264	4	4	
265	5	5	
266	6	6	
267	7	7	
270	8	8	
271	9	9	
272	:	:	
273	;	;	
274	<	SHIFT <	
275	=	SHIFT =	
276	>	SHIFT >	
277	?	SHIFT ?	
300	@	SHIFT @	
301	A	A	
302	B	B	
303	C	C	
304	D	D	

Table 2-3. (continued)
Teletype Code

Octal Code	ASCII Character	Key Combination	Remarks
305	E	E	
306	F	F	
307	G	G	
310	H	H	
311	I	I	
312	J	J	
313	K	K	
314	L	L	
315	M	M	
316	N	N	
317	O	O	
320	P	P	
321	Q	Q	
322	R	R	
323	S	S	
324	T	T	
325	U	U	
326	V	V	
327	W	W	
330	X	X	
331	Y	Y	
332	Z	Z	
333	[	SHIFT K	
334	\	SHIFT L	
335	]	SHIFT M	
336	↑	SHIFT ↑	
337	←	SHIFT ←	
340-373*			Lower case letters; codes cannot be generated from keyboard and should not be used in programs for reasons of compatibility
374	ACK		Acknowledge; code cannot be generated from keyboard and should not be used in programs for reasons of compatibility

Table 2-3. (continued)
Teletype Code

Octal Code	ASC II Character	Key Combination	Remarks
375*	①	ALT MODE	May be used for any desired control purpose
376*	ESC		Escape; code cannot be generated from keyboard and should not be used in programs for reasons of compatibility
377*	DEL	RUB OUT	Delete
		REPT	Causes any other key that is struck to repeat continuously until REPT is released
		HERE IS	In local, punches 20 lines of tape feed
		BRK RLS	Not connected

At the right end of the second row from the bottom is the repeat button (REPT). Pressing this button and striking any character key causes transmission of the corresponding code so long as REPT is held down. Characters that require the shift key may also be repeated in this manner, but there is no repetition of control characters. Pressing HERE IS (top row, right end) with the unit in local punches 20 lines of tape feed.

2.4.1 Tape

The tape moves in the reader from back to front with the feed holes closer to the left-hand edge. To load tape, set the switch to FREE, release the cover guard by opening the latch at the right, place the tape so that the sprocket wheel teeth engage the feed holes, close the cover guard, and set the switch to STOP.

To load tape in the punch, raise the cover, feed the tape manually from the top of the roll into the guide at the back, move the tape through the punch by turning the friction wheel, then close the cover. Turn on the punch with the unit in local and punch about two feet of leader. Code 200 or 377 can be used for leader or trailer. Press the CTRL, SHIFT and P keys to generate 200 (null); press RUB OUT for 377.

2.4.2 Paper

The printer may be either a sprocket feed or friction feed and uses 8-1/2 in. x 11 in. fanfold form paper or 8-1/2 in. roll paper. The roll supply is held in a tray at the back of the unit and printed forms can be torn off against the edge of the glass window in front of the platen. To replace the paper, first remove the upper cover by pressing the cover release button on the right-hand side. To free the remaining old paper for removal, lift the paper guides by pushing the handle marked PUSH at the right of the platen. To insert new paper from the tray, bring it up below the platen at the rear, line up the

holes at the edges of the paper with the sprockets, and press line feed (in local) to draw the paper under the platen.

NOTE

Paper guides and sprockets do not exist on friction feed version.

2.4.3 Ribbon

Replace the ribbon whenever it becomes worn or frayed or the printing becomes too light. Disengage the old ribbon from the ribbon guides on either side of the type block, and remove the reels by lifting the spring clips on the reel spindles and pulling the reels off. Remove the old ribbon from one of the reels and replace the empty reel on one side of the machine; install a new reel on the other side. Push down both reel-spindle spring clips to secure the reels. Unwind the fresh ribbon from the inside of the supply reel, over the guide roller, through the two guides on either side of the type block, out around the other guide roller, and back onto the inside of the takeup reel. Engage the hook on the end of the ribbon over the point of the arrow in the hub. Wind a few turns of the ribbon to make sure that the reversing eyelet has been wound onto the spool. Make sure the ribbon is seated properly and feeds correctly in operation.

2.4.4 Tabs

Each tab mechanism, horizontal and vertical, is a slotted wheel surrounded by a spring on which are mounted a number of tab stops. The slotted wheel for the horizontal tab is mounted on the spacing drum, and the tab can be set by inserting a tab stop in a groove where it catches the tabulator pawl when the type block carriage is in the desired position. With needle nosed pliers, lift the tab stop out of the slot in the wheel against the spring tension. Slide the stop along the spring in the desired direction and reinsert it into the slot at the new location. A stop may be removed from use by turning it so that it does not catch the pawl. The slots in the disc of the vertical tab mechanism allow tabs at any desired lines, but adjacent tabs must be at least an inch apart.

CHAPTER 3
SYSTEM LOGIC

In addition to presenting a detailed description of the logic of the PDP-8/S and the Teletype ASR 33, this chapter explains the organization of the drawings and the conventions used in them that represent that logic.

3.1 DRAWINGS

There is a complete set of electrical drawings, consisting primarily of D-size flow charts and logic drawings (block schematics) that accompany each PDP-8/S. Every drawing is labeled with a DEC drawing number in five parts, such as D-BS-8S-0-14. The first part is a letter indicating the size of the drawing; the second is a mnemonic code indicating the type of drawing; the third is the type code of the equipment (8S for the computer, PT08 for the teletype); the fourth is the drawing serial number (see next paragraph); and the last is a number specifying the individual drawing. If a drawing includes several sheets, both the sheet number and the number of sheets are written at the lower left of the drawing number. If a drawing is revised after being signed by the project engineer, a revision letter is written at the right.

Some typical drawing type codes are BS (block schematic), BD (block diagram), FD (flow diagram), TD (timing diagram), MU (module utilization), ML (master drawing list), PL (parts list), CL (cable list), WL (wiring list). The last four codes are usually A size.

Numbers on drawings of individual circuits are of essentially the same form based on the circuit type number. These are usually B or C size and are drawing type replacement schematic (RS). At the right of the drawing number there may be a letter or number that indicates a revision of the drawing. At the left or below the drawing number, there may be a letter or number that indicates a revision of the printed circuit.

Almost all of the drawings included in this manual are flow diagrams, logic drawings, and circuit schematics. (Appendix 1 describes the other types of engineering drawings and their use.) Drawings in the manual are intended for instruction purposes only, so persons working at the machine should use the prints that accompany the equipment rather than the figures in the manual. Drawings printed in the manual are serial 0, corresponding to the standard production machine. Although every computer is assigned a different serial number, most of the prints accompanying the equipment have drawing serial 0. But if a particular computer differs in some way from the standard machine, those drawings that reflect the difference have the same serial number as the lowest numbered machine that is so modified. Therefore, although the manual drawings are complete for the standard computer, maintenance personnel should use the separate prints for work on the equipment because they show any variations peculiar to the installation.

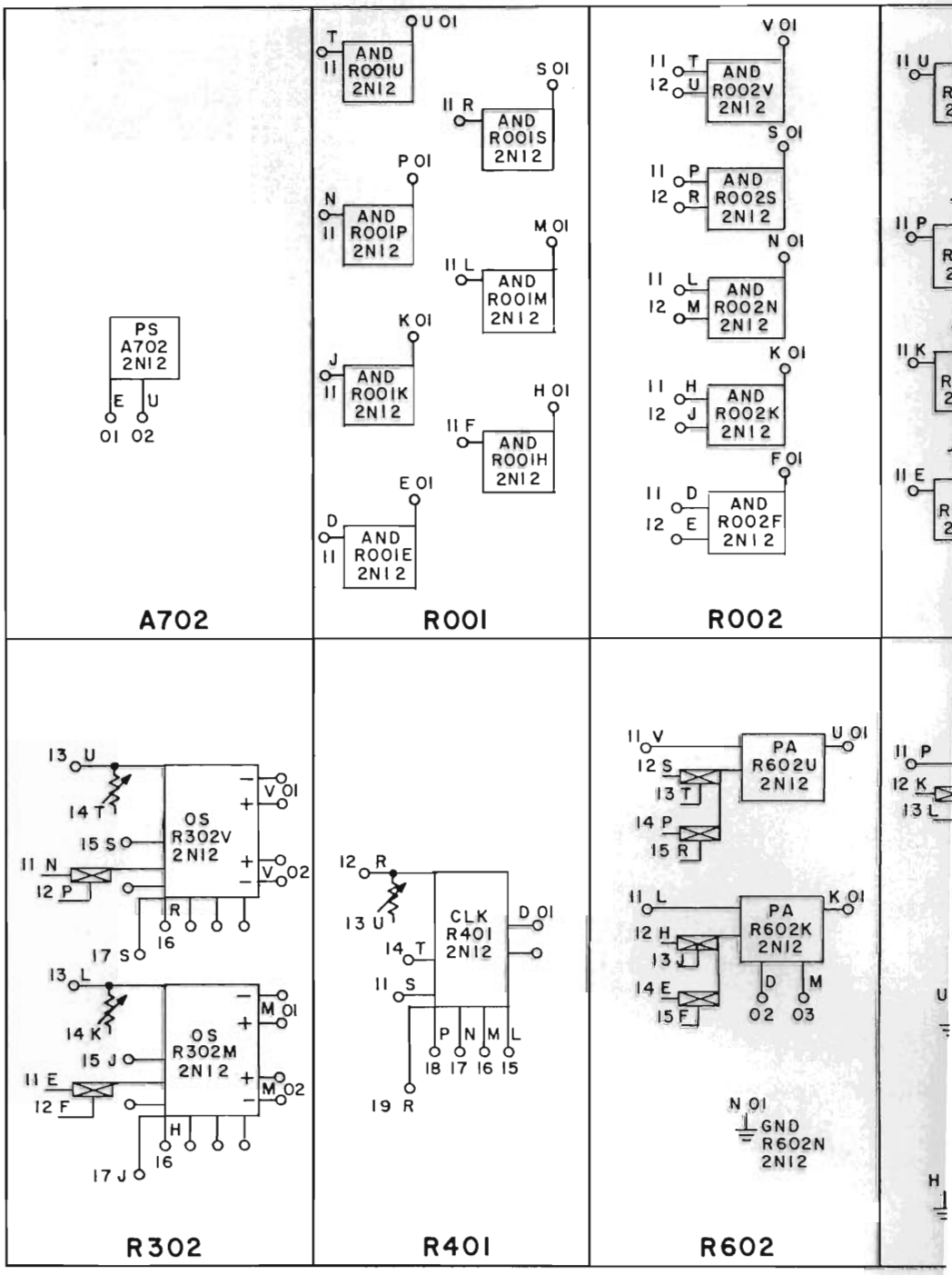
At the back of this manual the circuit schematics are in order by circuit type number, and the remaining drawings are in order by individual drawing number, i.e., they are ordered by the last part of the drawing number, and it is these individual numbers that are used for reference throughout this chapter. Hence the drawing (D-BS-8S-0-14) mentioned above is variously referred to in the text as print 14 or drawing 14.

3.1.1 Logic Drawings

The logic drawings are block diagrams that show the function of every logic element used in the computer. They also indicate the signal present at any module connector pin that carries a logic signal or some special voltage. The standard power and ground pins (A to C on every module) are not shown. In addition to giving the function of every logic element, the drawings identify every circuit by type number as given in the DEC Logic Handbook followed by the letter for the output pin of the particular part of the circuit used. Below the type number is a location code made up of one digit, one letter and two digits. For example, the location code 1 B29 represents module connector 29 in mounting panel B (all location codes begin with a redundant 1 -- the entire computer is contained in a single group of mounting panels). Pin designations are formed merely by adding the pin letter to the location code. Note 1 B29D. Some modules are double height and have two connectors. On the circuit schematic, A and B preceding the pin letters indicate the upper and lower connectors respectively, but on the logic drawings the prefixes are the appropriate mounting panel letters. Taps (if any) located on the handle end of the module are numbered. In the lettering on the drawings, the numeral 0 has a slash through it (Ø) to distinguish it from letter "O".

By convention, a logic level is regarded as true when negative (-3 Vdc) and false when ground. If a line carries a logic level that represents some logic function X, then the line is labeled X if it is negative when X is true, but is labeled -X (not X) if it is ground when X is true. It is easier to regard pulses as timing functions rather than logic functions, but for consistency a positive-going pulse is regarded as false and the line carrying it is so labeled. These conventions apply to all but the teletype drawings, whose conventions are explained with the description of the teletype in the last section of the chapter.

Figure 3-1 shows the symbols used to represent the logic circuits on the block schematics. Information about these circuits is given in the DEC Logic Handbook, but the system of diamonds and triangles used there to show signal type and polarity is not used here. All blocks are labeled to show logical and/or electrical function, except flip-flops which can easily be recognized by the form of their representation and are named according to their use or the meaning of the information they contain. Logic gates are labeled from the point of view that negative is true. Inputs are at the left of a block, and outputs are at the right or top. Signal names are written slightly above horizontal lines or their extensions.


PS
A702
2N12
E
U
01 02
A702
T
11
AND
R001U
2N12
U 01
S 01
11 R
AND
R001S
2N12
P 01
N
11
AND
R001P
2N12
M 01
11 L
AND
R001M
2N12
K 01
J
11
AND
R001K
2N12
H 01
11 F
AND
R001H
2N12
E 01
D
11
AND
R001E
2N12
R001
V 01
11 T
12 U
AND
R002V
2N12
S 01
11 P
12 R
AND
R002S
2N12
N 01
11 L
12 M
AND
R002N
2N12
K 01
11 H
12 J
AND
R002K
2N12
F 01
11 D
12 E
AND
R002F
2N12
R002
13 U
14 T
15 S
11 N
12 P
17 S
OS
R302V
2N12
V 01
V 02
R
16
13 L
14 K
15 J
11 E
12 F
17 J
OS
R302M
2N12
M 01
M 02
H
16
R302
12 R
13 U
14 T
11 S
19 R
CLK
R401
2N12
D 01
P N M L
18 17 16 15
R401
11 V
12 S
13 T
14 P
15 R
PA
R602U
2N12
U 01
11 L
12 H
13 J
14 E
15 F
PA
R602K
2N12
K 01
D M
02 03
N 01
GND
R602N
2N12
R602

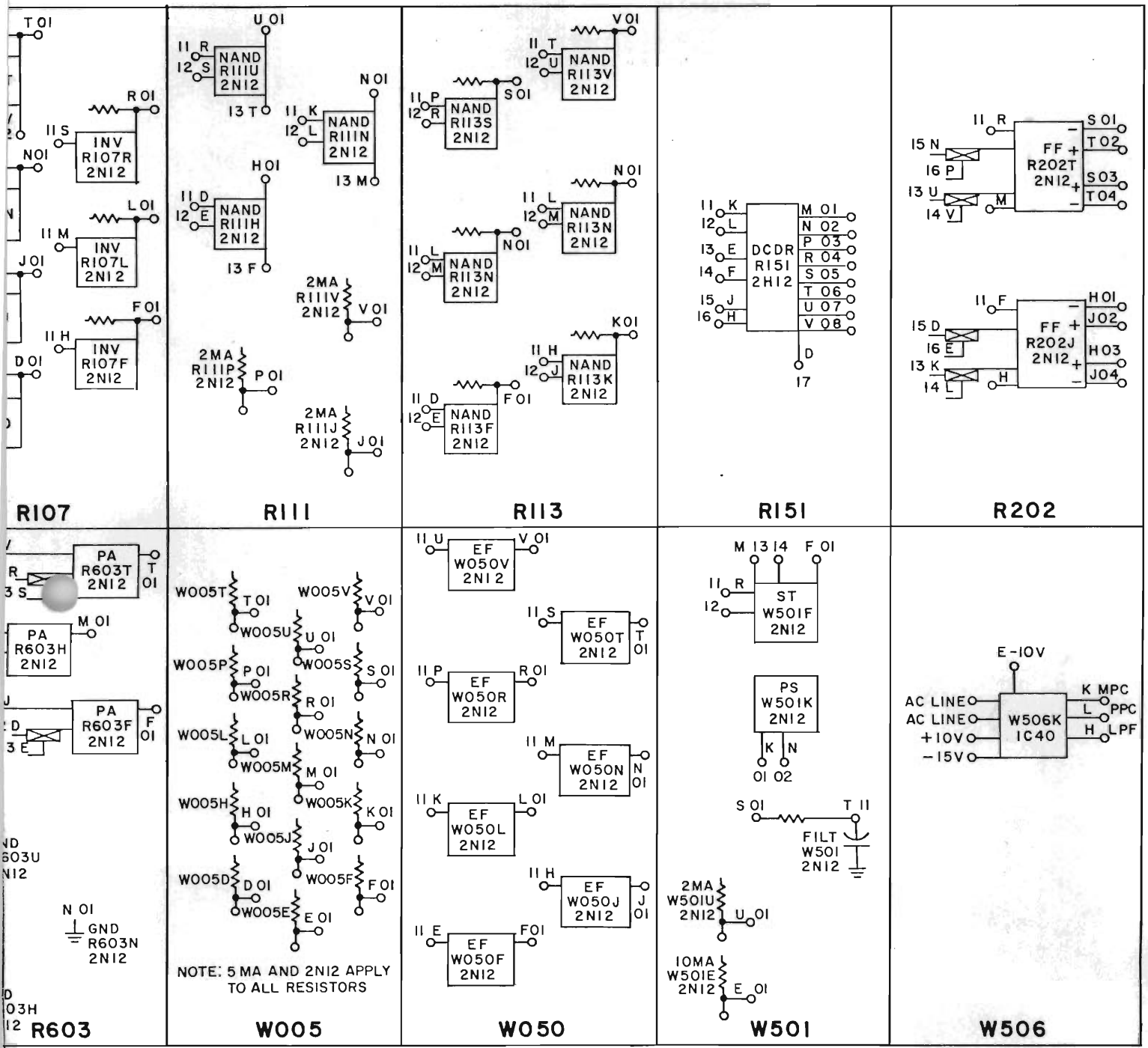


Figure 3-1 Logic Symbols

Each NAND gate actually has two parts, a diode AND gate and an inverter. The nodes shown below the blocks for the R111 gates are points at which other AND gates can be connected in conjunction with the AND part of the R111. The 0 and 1 inputs to the R151 decoder receive signals, wherein a negative level represents the state of a binary source, i.e., if the signal X is applied to pin L, -X must be applied to K. The single output selected by a given input configuration is at ground provided that the enabling input D is also at ground.

The diode-capacitor-diode input gate used with flip-flops, one-shot delays, and pulse amplifiers requires a ground-enabling level, and the triggering input to the DCD gate, as well as direct triggering inputs to the circuits, require positive-going pulses or level changes. The R401 clock produces a pulse train, and a negative enabling level is present at S. PA and clock outputs are positive-going 100-ns pulses, but one of the PAs on R602 produces 400-ns pulses if D and M are jumpered.

If a pulse is applied to both input gates of a flip-flop while both are enabled, the flip-flop complements. A flip-flop can also be set or cleared by grounding its 0 or 1 output, respectively. Note that on the symbol representing a flip-flop (and also the one shot), the output terminals are drawn twice using signs to show the polarities associated with either state of the circuit. They are drawn in such a way to eliminate excessive line crossing in showing the shift connections from one bit of a register to another, and also for ease in recognizing the required state of the flip-flop in cases where connecting lines are drawn directly from its outputs to other circuits on the same print. Nominally, the 1 and 0 outputs are those so labeled on the circuit schematic, these being the ones shown as negative beside the 1 and 0 in the illustration. In the logic drawings, however, the output names are reversed whenever the logical configuration is simplified by doing so.

The W501 is a Schmitt trigger circuit that produces a standardized logic level change from a switch closure. The W506 is a monitor that generates clear levels at power turnon or failure. The remaining circuits illustrated do not take part in the actual logical flow of events. The A702 is a -10V reference supply in the memory, the W005 contains clamped loads, and the W050 contains emitter followers to drive indicators. An emitter follower output is always labeled only by the pin to which it is connected. It never has a logical name.

Occasionally, in the text and flow charts, the location of a circuit on a block schematic is called out by rectangular map coordinates. Each drawing has eight columns numbered from right to left and four rows lettered from bottom to top.

3.1.1.1 Signal Notation. - Signal names are usually mnemonics that indicate the function or meaning of the signal. Composite signals sometimes have short names indicating function, but usually a composite is named by the entire logical function it represents, with a plus sign indicating logical OR and an asterisk indicating AND. Every flip-flop has a name which is also the name of its 1 output; the same

name preceded by a minus sign specifies its 0 output terminal. A minus sign applies only to the term it precedes unless parentheses are used to group terms.

Associated with every register is a shift pulse that shifts the contents of the register to the right and whose name is the name of the register followed by the letters SH. The name of the shift input to the left end of the register is the name of the register preceded by the letters RI "(readin)". Numerals that represent register bits are merely appended to the register name. For example, bit 11 in PC is PC11. Outputs of the flip-flops in some registers are buffered, and the buffer outputs are named by the register name preceded or followed by a B. In the case of MB and the word-time flip-flops, the direct outputs are used only locally (e.g., as the bit-to-bit shift levels in MB), so the flip-flop names are assigned to the buffer outputs rather than the actual outputs of the flip-flop circuit. Therefore, the logic signal WTD is actually the output of an inverter driven from the 0 output of the WTD flip-flop.

With only a few exceptions, the source of any signal, i.e., the drawing that shows its generation, is obvious from its name. Any signal that contains the name of a register is generated on the drawing that shows the register, and any signal that begins with BT originates on the drawing that shows the bit timing. Table 3-1 lists the various mnemonic codes, their meanings and the drawings associated with them.

Table 3-1.
Mnemonic Index

Code	Print	Meaning
A	11	Basic time pulses generated by bit timing
AC	20,10	Accumulator
BT	11	Bit timing
IC	5	Information collector
IO	17	In-out
IR	16	Instruction register
L	20,10	Link
MA	12	Memory address
MB	9	Memory buffer
MEM	22,23 4,18	Memory (8K) Memory (4K)
PC	19	Program counter
S	14	Sum output of adder
WT	13	Word timing

AC and L are shown together on drawing 20, and some of the control signals for both are on print 10. Any composite signal that begins with an instruction mnemonic originates on the instruction register drawing; the parity logic is shown with MB; the skip control flip-flop (SKP) is on print 10; and the various functions originating from console keys and switches are on print 15.

3.1.2 Flow Charts

Drawings 29 and 30 are flow charts of all operations that can be executed by the PDP-8/S and the teletype. These figures show every event, and insofar as possible, show the flow of operations in a manner that is equivalent to the actual gating and timing in the hardware. The terminology is from the logic drawings unless italicized.

Except for connections from one line to another or a return loop, flow in time is always down. A pair of horizontal lines breaking a vertical line indicates a delay; between the lines is listed the delay time, or the condition that must be satisfied to continue the flow. Pulses always appear in ellipses and events or level assertions in rectangles. For more complete correlation with the logic drawings, an empty ellipse indicates a pulse amplifier whose output has no name. A condition written on a line must be satisfied for flow to continue along the line. When several vertical lines branch from a horizontal line, the conditions are written above the vertical lines. To follow the chart, the reader must realize that at any branch point the flow continues on all lines whose gating conditions are satisfied.

In several cases the same event occurs in a number of flow lines, and such an event is often controlled by a composite function which may or may not have a simple mnemonic name. These composite functions seldom appear on a flow line because they are satisfied by the lesser conditions associated with the individual line. In other instances, instruction mnemonics appear as gating conditions, whereas the gating levels in the logic may be the combination of several terms that taken together represent the instruction. In any event, every composite function that appears in the logic drawings with a distinct name (that is not written merely as a combination of all its terms) is written on the chart, usually near that part of the flow in which it plays a role. Note that the logic functions SKIP and OP SKIP are used on the flow charts for convenience only. They do not appear on the logic drawings.

Drawing 30 shows the main flow including all word times and all operations executed from the console. The loop in the upper left-hand corner represents the processor clock, which is always in operation unless the word time has been stopped for a memory cycle. The clock output does not operate the processor, however, unless RUN has been set in one of the lines of flow that originate from console keys, as shown in the upper right. The remainder of the chart shows the many operations that occur at the different word-time pulses in all of the instruction word-times, the break word-time, and the word-times executed for the console functions Load Address, Deposit, and Examine.

The main line is the vertical one at the left, originating in the clock loop. The first horizontal line to the right is merely for a clear function at power turnon or power failure. While RUN is set, the clock output produces the basic A pulses that generate the bit time functions by shifting the timer T. The remaining lines to the right represent the generation of the bit time pulses. The first line represents only the first pulse in each set of fourteen and it is used only for special functions including entry into the in-out sequence, which is shown in a separate flow chart in the lower left on print 29. The special sequence shows the events associated with IOTs for the processor, and the right two-thirds of the drawing contains detailed flow charts of input and output teletype operations.

The pulses triggered in the third line to the right occur only at the first two bit-times and are used only for right rotation. The next line stems from the first twelve bit-times, and it is this set of twelve pulses that controls the processing of full words for all information transfers, addition, logic functions, incrementing, and testing conditions for skips. The next line represents the thirteenth bit time, and its pulse A12 triggers individual events that are required for certain operate instructions, checks parity, checks for overflow in addition, triggers a memory cycle whenever one is required, and stops the computer on a programmed or operator halt. Calling a memory cycle stops the clock, and flow continues to the memory chart in the upper left on print 29. The bottom line represents the final bit time, which controls the selection of the next word time.

Note that in the flow chart all gating conditions are written as logic functions without regard to truth values associated with voltage levels. In other words, an event that occurs in the fetch word-time is gated by WTF, whereas the actual gating level shown in the logic drawings may be a negative level labeled WTF or a ground level labeled -WTF. Similarly, the reader can easily determine whether a level in the logic labeled -X causes an event to occur when X is true or when X is false by consulting the equivalent representation of the logic in the flow chart.

3.2 TIMING

The timing for processor operations is in two parts, the generation of the bit-time pulses to control the sequence of events in each word time, and the selection of the different word-times to control the overall execution of computer instructions, breaks, and console functions.

As can be seen at the top center of the main flow chart (drawing 30) every pulse from the clock complements a flip-flop that is shown at C4 in logic drawing 15. Every time the flip-flop clears, it triggers a series of clear pulses for the logic if the processor power clear level is true. The turnon of this level also clears other control flip-flops, places the computer in fetch time, and resets the timer to its initial state. The PPC level comes from the power monitor, shown at bottom center on drawing 17. This circuit monitors the +10V and -15V logic supplies and the -10V memory reference. It produces power-clear signals for both memory and processor whenever any voltage is not within its proper range. At power turnon, both clear outputs remain at ground until about 50 ms after the last voltage threshold

has been met to allow any motors, solenoids, relays, and the like, to reach operating conditions. Then MPC goes off (-MPC drops to -13V), and about 5 ms later PPC turns off. Whenever any voltage fails to maintain its proper value, the outputs remain negative for 9 to 16 ms, at which time PPC turns on, clearing the processor and 3 to 10 ms later MPC clears memory control.

The power monitor module also contains a low power condition flag (LPC), which can be used to restart the computer automatically, following a power failure. In 3 to 6 ms after any voltage failure LPC sets, and this state change requests a program interrupt if the interrupt is enabled. In this way, before the power-clear levels turn on, the program has at least several milliseconds in which to store the various processor registers in memory and place an appropriate jump in location 0. After the power-clear signals go off (power is restored), LPC clears, restarting the computer at location 0, if the optional auto restart circuit (W501 in 1E5) is in the machine. The auto restart is disabled by removing this module.

3.2.1 Bit Timing

Print 11 shows the clock, the timer or time ring counter T, and logic that decodes the counter to generate the bit time functions and pulses. The clock at the upper left generates a pulse train except when WTS is set to stop the word time for a memory cycle. So long as RUN remains set, the pulse train triggers the A pulses which rotate T to the right. The input gating levels to T0 are reversed from those for the other bits, so each shift places the complement of T6 in T0.

The initial pulse in Load Address, Deposit or Examine resets the timer to its initial state. The RT pulse is applied to the common set input (M) of the last two bits at the right, but the 0 and 1 sides of T5 are reversed, so only T6 is set. All remaining bits are cleared. The same configuration is produced by power clear.

From its initial state with a 1 in T6, the A pulses fill T with 1s from the left until it is all 1s, then 0s come in from the left until it is clear. The generation of bit-time levels from the T-states is shown in the upper left of the flow chart, and the generation of bit time pulses is listed on the logic drawing. A given bit-time level conditions the logic to produce a time pulse having the same number, but the pulse also steps the counter to the next bit time. For example, when T is clear, BT00 is true and the next A-pulse generates A00, but this same pulse sets T0, thus generating BT01. Note that the initial state of the timer actually corresponds to the final bit-time in a processor cycle, so the first pulse is actually A13, which selects the proper word-time to enter. Every A12 should automatically produce this state, but A12 triggers the reset pulse to force the state and prevent any malfunction from disrupting more than one cycle. Note also that the initial pulse in the console operation start clears T6 so that the computer starts at the beginning of a word time. It is assumed that the operator will press the start key only when the timer is in its initial state and hence all other bits are clear.

The logic on the left-hand side of drawing 11 decodes the register for the bit-time levels that serve as gates for the PAs to generate the time pulses. The top PA generates a pulse only at the beginning of each word time, the second PA produces a pair of pulses for the first two bit times. Individual pulses produced during the last two bit times, 12 and 13, and a string of 12 pulses for the basic word processing is produced while BT (00-11) is true. The main string and A12 are combined to produce a string of 13 A (00-12) pulses to control the carry flip-flop during addition. The remaining gates generate two BT levels, each of which is true during part of the basic processing time, to control the transfer of an address to MA after each instruction is fetched (the instruction word specifies only a 7-bit address).

3.2.2 Word Timing

The column of flip-flops at the center of drawing 13 controls the execution of the various word times except for console functions. The third flip-flop from the bottom, AI, specifies whether an instruction addresses an autoindexing location. At the end of each word time, the nets at the left of the flip-flops determine which word time must be entered next, and A13 triggers the transition by clearing any WT flip-flop that is set and setting the appropriate one for the next word time. The direct outputs of the WT flip-flops drive only inverters whose outputs in turn are used for all logic connections; the flip-flop names are applied to these buffered outputs. (The names do not reflect the fact that the signals are buffered.)

The logic net at the left of AI grounds the enabling level for the AI set gate if the left half of MA is clear. Bits 5 through 7 of MB are clear and MB08 is 1. The appearance of this configuration in the fetch time of an instruction that calls for indirect addressing indicates that one of the autoindexing locations, 10-17, is being addressed. Of course AI is set at A12 in any word time in which this particular configuration exists, but its being 1 is used to control the selection of index time only when such selection is possible.

The final pulse in every word time, A13, always clears AI, but it is applied to both set and clear gates of all other flip-flops. The level inputs to the clear gates are grounded and therefore always enabled, but the gating levels for the set inputs come from logic nets that determine which word time the computer must enter next. Since no word time ever follows itself, the set inputs are enabled at only one, or at most, two flip-flops and these must presently be clear. Pulse A13 clears any flip-flop that is presently set, and sets only the ones appropriate to the next word time. State changes in the flip-flops are shown in detail at the bottom of the main flow chart (print 30).

During any word time in which the processor must deposit a word in memory, the net in D3 of print 13 pulls the -WTWR level false. A similar net in B6-7 grounds -WTRD in any word time that must retrieve a word from memory. If either type of memory cycle is necessary, A12 triggers the memory request pulse MR through the PA in the ~~lower~~ center left-hand corner of the drawing. This pulse triggers one or the other of the two PAs just to the right to start a read-write or a clear-write memory cycle depending

upon whether reading or writing is required. MR also sets WTS (B3) to stop the word time by stopping the clock. At the end of the memory cycle, the MEMGO level goes false, clearing WTS and allowing the clock to proceed to A13.

The AND gates hung on the outputs of WTS, WTE, and WTF set or clear these flip-flops for various console operations and power clear. The direct set and clear inputs to all of the flip-flops are also used for this purpose. The remaining logic nets at the right-hand and the upper left-hand sides of the drawing generate various composite control levels whose names in all but two cases are written out. WTINCPC at the upper left (D6) gates PC into the adder whenever it must be incremented; WTINCR inputs a 1 to the adder whenever any register is being incremented.

3.3 REGISTERS

The registers in the computer are used in different ways, and their names reflect their use. But regardless of their use they all function in essentially the same way. All are shift registers in which one bit is connected to the next for right shifting. In a few cases, the direct set and clear inputs to the register flip-flops are used either to clear a register or to effect a parallel transfer (as from the switch register to AC), but there is no complicated input gating for producing logical or arithmetic functions or parallel transfers from various sources. Whenever the contents of any register change or are transferred to another register, information is shifted to the right in all registers affected. Information from a register is made available only one bit at a time at the right end (LSB), and information is shifted into a register only one bit at a time at the left end (MSB). A register clears if it has no input while it is shifting, but often the input to a register is its own output, so the contents of the register are recirculated while it is supplying information to some other register. All registers except IR have 12 bits, but AC and the link often function together as a 13-bit register. IR has only four bits.

3.3.1 Instruction Register

The register that holds the instruction code and indirect bit during the execution of each instruction is shown in the upper left-hand side of drawing 16. IR is cleared only in special circumstances, such as at the beginning of a console operation or a program break. After each instruction is fetched from memory, the contents of MB are shifted into IR by the standard 12-bit shift, which therefore leaves the left four bits of the word in IR and drops out the address part at the right.

The R151 at the right decodes the left three IR bits to determine the instruction; one of the decoder outputs is always at ground to specify some instruction except when an Examine or Deposit is being executed. IR03 is combined with the two states of AI to select indirect addressing with or without autoindexing. At the lower left (A7) the OPR level is combined with the two states of IR03 to determine the operate group. The OP1 level is then further combined with bits from MB to determine the specific operate instruction. The remaining nets generate composite functions to control events common to more

than one instruction or to determine specific conditions within one or more instructions, for example, to determine whether the count is zero in an ISZ (ISZ·ZI) or to determine the circumstances in which PC must be incremented an extra time.

The meanings of the functions generated are obvious except for the rotate levels at the right. ROTR is true during right rotation (OP1 · MB08) when either MB10 is true or the processor is not in the first bit time (BT00 is false). This level gates the A(00-01) pulses for the right shift so there can be at most two shifts. If a 1 is programmed in instruction bit 10, both shifts occur, but if bit 10 is 0 there is only one shift at BT01.

There are no gates for left shifting, so a left rotation is produced by a shortened right shift. AC and L are rotated together, so a complete rotation would require 13 shifts. Since the right shifting for a left rotation occurs on A(00-11), there are at most 12 right shifts (the result is at least one left shift). The shifting is controlled by ROTL which is true during left rotation (OP1 · MB09) when either MB10 is false or BT00 is false. If a 1 is programmed in bit 10 of the instruction, ROTL is true except during BT00, which eliminates one of the 12 right shifts.

3.3.2 Memory Buffer

Because MB is the buffer between processor and memory (print 9), the entire register is cleared at the M pins by a request for a read-write cycle, and the parallel transfer of a word read from memory is effected by memory output pulses that set individual MB bits. Pressing the start key also clears the register. Direct outputs of the MB flip-flops are used only for shift gating within the register; all remote connections use the inverted outputs whose names do not reflect their being buffered from the register bits. An extra set of buffered outputs for the in-out bus supplies both sides of the center six bits for device selection and the 0 sides of all bits for output in a data break (optional equipment).

The two logic nets in the upper left generate the MB shift pulses and the shift inputs to MB00. MB can receive information from PC or AC for deposit in memory, from the adder during an indexing operation, and from itself while it is being made available to IR and MA in fetch time (-WTS holds off the MB level during memory access). Note that the bottom two gates in the enabling net for the shift pulses are satisfied simultaneously in AND, TAD, and JMP, in which the execute and end times are performed together. In these two word times, input is supplied to MB in only three cases (DCA, ISZ, JMS). Otherwise the gates clear MB except when its contents are needed for the instruction (device selection in an IOT, selecting operations in an OPR).

3.3.3 Program Counter

This register (print 19) receives an address from MA during a jump instruction. It receives the output of the adder when it is indexed in fetch time (Examine and Deposit) when it receives address 0001 in break time, and when it receives an address from the switch register via AC and the adder in

Load Address. During end time, it receives the sum from the adder whenever any extra indexing is required (a skip or a JMS), but recirculates itself in all other instructions except JMP in which it receives MA because WTX and WTE are simultaneous.

3.3.4 Memory Address

Drawing 12 shows the register whose 12 bits select one of the 4096 locations in memory during a memory cycle. At the lower right-hand side of drawing is the page zero flip-flop, which is set by the first pulse in fetch time if bit 4 of the instruction is 0. The shift input nets at the left supply the 7-bit address from MB for the first seven fetch pulses, but recirculate the original contents of MA00-04 in the rest of the word time unless PGZ has been set, in which case the input is inhibited and MA will address page 0. MA receives a 12-bit address from MB in defer time, receives PC for a memory access in Examine or Deposit, and recirculates itself while its contents are being transferred to PC in a jump. In end time, except in JMP, it receives an address for the next instruction retrieval from PC, either directly or incremented by one through the adder. The direct inputs are not used, and the register is cleared only when shifted without input in break time.

3.3.5 Accumulator and Link

AC and L, both shown on print 20, have separate control pulses, but the two function together as a 13-bit register when used for addition or rotation. All 12 AC bits are cleared at once by two of the operate instructions, by an IOT, by power clear, and by any console operation except Continue. To load information from the switch register into AC during Load Address (Deposit or OSR) the logic at the top of print 10 generates the SAC pulse which sets individual AC bits through any switches that are on. AND gates tied to the 0 AC outputs allow pulses from the information collector to effect a parallel transfer into AC from the in-out bus. Buffered AC outputs drive the bus for transmission of information to peripheral equipment.

The shift inputs to AC are produced by the net on the upper left-hand side of print 20, and the shift pulses are generated by the logic in the lower left-hand side. Most shifting is produced by the standard set of A(00-11) pulses (although ROTL may eliminate one of these), but there is an additional shift at A12 in the TAD execute time to complete the 13-bit addition, and one or two shifts may be generated at A(00-01) for right rotation.

During a rotate instruction, the link (at the center left of the drawing) receives information from AC, and AC in turn receives it from L. In TAD, L receives the sum and AC receives L. In IAC or CMA, both AC and L receive the adder output but at different times: in IAC, L complements at A12 if the AC incrementing has produced a final carry (has overflowed); AC is complemented through the adder in CMA, but the CMA input to L is redundant and L merely shifts into itself. The word shifted into AC in AND is the bit-by-bit AND function of the contents of MB and AC. AC recirculates itself

while being shifted to MB in Deposit (the Examine shift is redundant), and it receives its original contents through the adder during OP2 while being tested for zero contents.

Print 10 shows the generation of the control pulses for the link. LSH is generated at the same time as ACSH in those instructions that operate on AC and L together, except in IAC and CMA when LSH is at A12 only. In the upper part of the drawing (print 10) is the net that generates set and clear pulses for L in fetch time of those operate instructions that control it. L is cleared by an instruction that calls only for clearing or calls only for complementing and it is now set. It is set if the instruction calls for both clearing and complementing or calls only for complementing and L is now clear.

3.4 CONTROL CIRCUITS

Besides registers and timing logic, the processor contains a serial adder, parity and skip logic, and circuits associated with the console.

3.4.1 Adder

The serial adder (print 14) produces the sum of a pair of numbers one bit at a time. For each step, the circuit uses three inputs: two are bits from summands SX and SY (two numbers to be added), the third is the carry-in from the previous step (the carry into the first step is of course 0). At each step the address produces two outputs, a bit of the sum S, and the carry out C which is stored in CA for the next step. The outputs are generated in exactly the same way as one would when performing pencil and paper addition of binary numbers. S is true (that is, 1) if the sum is odd, if one and only one input is true or all three are true. The carry is true if the sum is 2 or greater, i.e., if any two inputs are true.

The upper net on the left-hand side of print 14 generates the input SX. This input comes from AC in TAD; but in any other case in which addition is actually performed, SX is true only during BT00 and hence has the effect of adding one to the number received as the SY input. BT00 is gated-in during Examine and Deposit to increment PC, and by WTINCR during any other operation that requires incrementing and also in break time to supply address 0001 to PC (there being no SY input at this time). When there is no SX input, the number shifted out at S is identical to that shifted in at SY. This procedure is used to complement AC, to test it for zero, and to transfer it to PC.

The number shifted into SY is from PC during Examine or Deposit, from MB in addition or indexing, and from AC during Load Address or the operate skip group. WTINCPC gates in PC for normal program counting in fetch time and for a skip or JMS in end time. The remaining gates control SY during the operate instructions CMA and IAC. The gates at the bottom bring information from AC (the left gate receives the complement of AC for CMA) except at BT12 when the top gate substitutes L. The CMA link shift is redundant, but in IAC, A12 complements L when there is a carry (overflow). Note that the gate for IAC, which is enabled by MB11, includes the condition -MB06; so when the program calls for both complementing and incrementing (CIA), the adder adds one to the complement (that is, forms the two's complement).

On the lower right-hand side of print 14 is the zero indicator flip-flop ZI, which is set by the final pulse in fetch time. It is then cleared if the sum is ever true in execute time of an ISZ or the operate skip group.

3.4.2 Parity Logic

On the upper left-hand side of the main flow chart is a small isolated flow diagram beginning with MBSH. It indicates that PG is complemented whenever a 1 is shifted into MB, and PT is complemented whenever the bit shifted out of MB is 1. These events occur whenever MB is shifted in any flow line. On print 9, PT is shown at the top and PG at the left-hand side. Both flip-flops start clear so that whenever MB is shifted, PT tests the parity of the word shifted out and PG generates an even parity bit for the word shifted in.

When a write request is made, A12 shifts PG into PB, which is written in memory with MB. For reading, the CMB pulse that clears MB also clears PB, which is then set if a 1 is read from the parity plane. Following the shifting of any word that has been read from memory (at the end of any word time that follows a read memory cycle), PE SET sets the parity error flip-flop PE if PB and PT differ (if the test bit generated from the word differs from the parity bit read from memory). PE can be cleared by an IOT but is cleared otherwise only by power clear, the start pulse, or the examination of a memory location from the console. Note that detection of a parity error does not change the contents of memory: the word read from memory, whether correct or not, is written back into memory before the test is made.

3.4.3 Skip Logic

The SKP flip-flop that is shown near the center of drawing 10 controls incrementing of PC in execute time for skipping. A skip pulse from in-out control sets the flip-flop directly. The large net at the left of the flip-flop generates the skip condition for operate instructions.

A 1 in bit 5 of the instruction tests for negative AC (AC00 set), a 1 in bit 6 tests for zero AC (ZI set), and a 1 in bit 7 tests for L set. The selection is made by three NAND gates associated with the selection bits in the instruction. The output of any gate corresponding to a 0 selection bit must be negative; a gate output can be ground only if the selection bit is 1 and the selected condition is true.

The complete skip condition appears at the ORed outputs of the two NAND gates in B4. Instruction bit 8 specifies whether the skip is to occur when the selected condition is true or false; hence the upper NAND gate receives MB08 and the output of the selection gates, whereas the lower NAND gate receives -MB08 and the inverted output from the selection gates. If a 0 is programmed in bit 8 and any condition selected by bits 5 through 7 is true (making the output of the selection net ground and its inversion negative), then both inputs to the 1F07U gate are negative and the gating level to the set input of SKP is ground. Similarly, if no selected condition is true, the output of the selection

net is negative; in this case if bit 8 is 1, the 1C07U gate receives negative signals at both inputs. Hence if any condition is satisfied and a 0 is programmed in bit 8, or all specified conditions fail of satisfaction and a 1 is programmed in bit 8, then A12 in OP2 execute time sets SKP. The 1 state of this flip-flop causes an extra indexing of PC during end time of an OPR or IOT.

3.4.4 Console

Print 15 shows the inputs to the system from the console, and the RUN flip-flop through which the console keys and switches start and stop the computer. In the upper left is a register of switches that allow information to be loaded into AC by passing the SAC pulse to individual AC bits. Below the register are the operating keys and switches, each of which can place a ground on a control line provided that the console key lock is closed; if the lock is open, the keys and switches are inoperative.

Closure of any key except stop generates a trigger pulse through the Schmitt trigger circuit at the lower right; the inputs from the deposit, however, examine, and load address keys are gated by RUN, so they have no effect while the computer is in operation. For Continue, TP sets RUN. For Start, TP produces a start pulse SP through the PA at the left of RUN provided that the processor is not stopped for a memory cycle. SP clears most of the computer logic through the PAs in the upper right, and its trailing edge sets RUN through a NAND gate 400 ns later.

For Load Address, TP triggers a pair of load pulses (LP and LPA) 1 μs apart (C3). A similar pulse pair is used for Deposit and Examine, but in this case, TP triggers a common first pulse (DP+EP) and the output of the one-shot triggers separate delayed pulses for the two functions. The delayed pulse in any of these three operations sets one of the flip-flops at the left to control its execution (these are the word time flip-flops for console operations). At the end of the single word time, A12 clears the flip-flops and clears RUN through the PA in B5 to stop the computer.

The net at the far left allows A12 to clear RUN in end time of a HLT. The gates at bottom center cause A12 to clear RUN in fetch time if the stop key or single instruction switch is on, but in any word time if the single step switch is on.

The Schmitt trigger and PA on the upper right-hand side of the drawing are for the optional restart feature after power failure. The clearing of the LPC flip-flop in the power monitor triggers the AST pulse, which starts the computer in the same way the trigger pulse does when the start key is pressed (A4).

3.5 MAIN FLOW

Now that the reader has an understanding of the way the registers and the timing and control circuits function, he should have no difficulty in following any instruction or console function in the main flow chart (drawing 30). A discussion of the flow of events in memory access, the special IOT sequence, and teletype input and output (drawing 29) is included with the descriptions of the corresponding logic in the three sections following this one.

3.5.1 Console Operations

Entry into the flow is always made by means of the console keys, as shown on the upper right-hand side of print 30. For Continue the trigger pulse merely sets RUN to start the computer in its present state.

For Load Address, Deposit and Examine, TP triggers pairs of pulses that place the processor in operation for one word time. The first pulse for all three clears AC, WTF and WTE, and resets the timer. LP additionally clears all word time flip-flops, IR and other control flip-flops. Each of the second pulses sets RUN and a flip-flop that controls the word time for the function. EPA also clears PE, whereas DPA and LPA transfer the contents of the switch register to AC.

Below the initiation of the three functions are the word times used by them. In Load Address, the 12 A(00-11) pulses shift the switch register address from AC through the adder to PC, clearing AC in the process. For the other two operations, the pulses shift PC to MA and index PC. For Deposit they also move the switch register word from AC to MB. After the shifting is complete, A12 clears whichever word-time flip-flop has been controlling the operation, clears RUN, and places the processor in fetch time. For the two functions that require memory access, A12 generates MR, which stops the clock by setting WTS and requests the appropriate type of memory cycle: clear-write to deposit information, read-write to retrieve it. In the latter case, the pulse that triggers the memory cycle also clears MB and PB to prepare them for receiving a word from memory.

Pressing the start key causes the computer to begin normal operation by retrieving the instruction in the location addressed by PC. The trigger pulse from the key generates the start pulse provided that a memory cycle is not now in progress. SP places the computer in end time, clears T6 so the clock will start at the beginning of the word time, and together with two more pulses shown in the same flow line, clears the in-out equipment, MB, AC, IR and most of the control flip-flops in the processor. Finally the trailing edge of SP sets RUN to start the clock. Pressing the start key while the computer is running merely restarts it at the location presently addressed by PC, except that it will not interrupt a memory cycle to do so.

After the reestablishment of the proper voltage levels following a power failure, the power monitor level, LPC goes negative, producing AST, which duplicates the action of the trigger pulse produced by pressing the start key.

3.5.2 Instruction Flow

The loop in the upper left-hand corner represents the clock which is always going except during memory access. If action at the console sets RUN, the pulse train from the clock produces the A pulses that sequence the timer to produce the various bit time functions. The flow follows one or more of the lines to the right, depending upon which BT function is true. Insofar as it is practical, the series of events that make up a single word time appear below one another in the drawing.

Events common to all word times are closest to the main vertical line at the left. The first 13 pulses each save the current carry in CA whether an addition is going on or not. A12 sets AI if an autoindexing configuration exists in the appropriate MA and MB bits, clears RUN if the single step switch is on, resets the timer, and sets the program interrupt request flip-flop if the interrupt system is on and there is either a parity error, a power failure, or an interrupt request over the in-out bus. A13 clears a number of control flip-flops in preparation for the next word time.

The special word times for Load Address, Deposit, and Examine have already been discussed above. Following Start, the processor executes an end time in which it moves PC to MA and requests a read-write cycle to retrieve the first instruction.

3.5.2.1 Fetch. - After an instruction has been brought from memory, A00 sets PGZ if bit 4 of the instruction word is 0. It also turns on the interrupt system if the preceding instruction was an ION. The full set of word processing pulses A(00-11) moves the instruction code and indirect bit to IR and indexes PC. The first seven of these pulses move the address from MB to MA, and the next five then either reestablish the current page number in MA or clear MA00-04, depending on whether PGZ is clear or set. If IR now contains the code for a group 1 OPR, A12 sets or clears L and/or clears AC if these events are specified. A12 also stops the computer if the stop key or single instruction switch is on, triggers PE SET to check the parity of the instruction word, and requests a read-write cycle to get a new address if the instruction is indirectly addressed or to get either a new address or the operand for AND, TAD or ISZ. The condition on the line leading to MR is the general one for any reading or writing, but on this line it is satisfied specifically by the three conditions for fetch, index, and defer time that are written just at the right.

If RUN is still on when the clock restarts, A13 clears WTF, sets ZI for possible use in the instruction, and puts the processor into the next word time. If the instruction indirectly addresses an autoindexing location, A13 sets WTI; for indirect addressing with AI clear, defer time follows. If the instruction is an OPR or an IOT, or uses a direct address, A13 sets WTX; and it also sets WTE if the instruction is an OP1 or a directly addressed AND, TAD or JMP.

3.5.2.2 Index. - This word time merely indexes the address contained in MB, checks its parity, and calls a clear-write cycle to put the incremented address back in memory. The processor then enters defer time.

3.5.2.3 Defer. - This word time moves the absolute address from MB to MA, checks its parity, and reads the operand if the instruction is AND, TAD or ISZ. The processor then enters execute time and enters end time simultaneously for an AND, TAD, OP1 or JMP.

3.5.2.4 Execute. - For an IOT, A00 triggers the special in-out sequence. For right rotation, A(00-01) shift AC and L together once or twice as required.

The main set of A(00-11) pulses produces whatever transfers are necessary for the six memory reference instructions. For example, TAD shifts MB to the Y adder input, shifts AC to the X input, and shifts the sum through L back into AC. In ISZ, the SX input is true only at BT00, so the number shifted back to MB from the adder is one greater than that shifted from MB to SY. If the adder output is ever true, ZI is cleared. Note that the events shown for JMP are not complete on the WTX line: the return of MA to itself while being moved to PC appears in the WTE line because it is controlled by end time, which is simultaneous with execute time in this instruction.

Any full word operation required for an OPR also appears in the WTX line for the main set of twelve shift pulses. IAC adds one to AC, CMA complements AC through the adder; if both occur together, the adder receives -AC but IAC still makes SX true at BT00. For left rotation, AC and L are shifted right either 11 or 12 times. For the test-skip group, AC is rotated through the adder, ZI being cleared if the sum is ever true.

Following the 12-bit processing, A12 performs whatever additional operations are required to complete the execution of the instruction. In TAD there is an extra addition step through the adder to put the 12-bit result in AC and complement L from its original state on overflow (the adder input at this time is L, which has been shifted through AC). AND, TAD, and ISZ check the parity of the operand retrieved from memory: ISZ, DCA, and JMS write the operand in memory. IAC also complements L on overflow (CMA appears in the gating condition but has no effect). For the skip group A12 clears AC if bit 4 of the instruction is 1, and sets SKP if the specified skip condition has been satisfied. Finally A13 sets WTE if the processor is not already in end time.

3.5.2.5 End. - For an OSR (a 1 in bit 9), A00 transfers the switch register to AC. A(00-11) determine the address for the next instruction retrieval. For a JMS or an ISZ or OPR skip, PC is indexed and the result goes to MA. If there is no skip and the instruction is not a JMP, PC goes to MA. For a JMP the simultaneous execute time is moving the new address from MA to PC, and the MA shift controlled by end time merely reestablishes MA.

A12 clears SKP, clears RUN on an HLT (a 1 in bit 10), and requests a read-write cycle to retrieve the next instruction. When the clock starts again, the processor enters fetch time if there is no interrupt request, but enters break time if PIR is set.

3.5.2.6 Break. - A00 clears IR and turns off the program interrupt by clearing INS and ION (hence the break now in progress cannot be interrupted). A(00-11) clear MA, shift the present program location from PC to MB, and place address 0001 in PC. Then A12 checks the parity of the instruction just retrieved but not executed, and requests a clear-write cycle to save PC in location 0000. The processor then returns to end time automatically to execute the instruction in location 0001.

3.6 MEMORY

The computer may have either of two memories that differ slightly in physical configuration. The so-called 4K memory is shown in prints 18 and 4; prints 22 and 23 are the equivalent drawings for the so-called 8K memory, which is really a 4K memory mounted on 8K planes (6-1/2 planes of 64 x 128 bit mats). Which memory is in a particular machine can be determined merely by checking the location of the stack (the 8K stack is long and thin, and is used in all machines serial 200 and up).

— This machine is serial 201. However it has a 4K stack. However, some boards have the 8K numbers!!

3.6.1 Memory Control

Prints 18 and 22 show the timing and control logic for the two memories, and a flow chart of this logic is on the upper left-hand side of print 29. The logic is the same for both memories, the two prints being identical except for module locations. The basic timing is supplied by the clock and ring counter shown at the bottom. At power turnon, the MPC level from the power monitor clears this counter, and in every memory cycle it shifts through its 12 states (as shown in the flow chart) returning to zero. The clock setting is approximately 2 mc for the 6.3-μs memory, slightly slower for the 6.5-μs memory.

At left center of the print a request pulse for either type of memory cycle temporarily turns on the MEMGO level, enabling the clock. The first shift from the clock sets A, which holds MEMGO on so that the cycle can continue. Before A clears, F is already set so MEMGO continues until the counter is back to zero. At this time it returns to ground, clearing the WTS flip-flop in the word timing logic, and thus restarting the bit timing clock.

The timing signals to the core logic are derived from the counter and the flip-flop made up of the two NAND gates with feedback in the center of the print. This strobe enable flip-flop is set by a request for a read-write cycle, but is cleared by a request for a clear-write cycle. The read level to the core logic is true during the 2 μs while BM is 1 and FM is 0. During the read period, the single counter state in which DM is 1 and EM is 0 generates the strobe pulse provided that the strobe enable flip-flop has been set. This pulse strobes the memory read outputs into MB; thus when the strobe is not enabled, the read portion of a memory cycle serves merely to clear the addressed location. During the write portion of the cycle, the timing logic generates inhibit and write levels, each of 1.5 μs duration, with the latter beginning and ending 0.5 μs after the former. The inhibit is on while AM is 0 and DM is 1, the write is on while BM is 0 and EM is 1.

3.6.2 Core Logic

Block schematics 4 and 23 show the modules associated with the stack. The 4-wire stack has 13 planes with one sense winding and one inhibit winding per plane. Selection of a single location in the 64 x 64 matrix is accomplished by selecting one each from among 64 X-windings and 64 Y-windings. The two prints are identical except for module locations, and each G607 and G608 in the 4K memory

is replaced by a single G609 in the 8K memory. References in the following paragraphs are to the 8K print with the 4K references given parenthetically wherever necessary.

A single Y-winding is selected by decoding MA00-05 in the W108's, shown above and below the stack. The equivalent circuits that decode MA06-11 to select an X-winding are on either side of the stack. The sense circuits are at the extreme left-hand side in the print, and the inhibit logic is at the right. The -10V reference is supplied to tap terminals 1 and 2 on all W108's via the G609's (G608's). The ground read and write levels from memory control are applied to the lower inhibit W108 at the right; this section of the module is actually independent of the inhibit logic, and the associated drivers are used to generate the negative read and write signals applied to the X and Y W108's.

To understand the decoding of MA to select a pair of X- and Y-windings that intersect at a single location, consider the selection of a single Y-winding by the circuits shown above and below the stack. The top W108 decodes MA00-02 to select a single driver whose two outputs are tied together and connected to one end of a set of eight consecutive Y-windings through selection diodes on part of a G609 (G607). The bottom W108 similarly decodes MA03-05 to select a single driver, but here the driver outputs are applied separately to the selection diodes in part of a G609 (G607). There are two diodes per line and each output of each driver is connected through one set of diodes to eight Y-windings, one from each of the eight sets of eight selected by the top W108's. When MA00-05 is 00, the 0 winding is selected by decoding MA00-02 to select windings 0 through 7 and decoding MA03-05 to select the first winding from each set of eight windings, 0, 8, 16,....

MA remains stable throughout a memory cycle so the same pair of drivers remains selected, but current flows only while the read or write signal is true. The read and write signals are connected to opposite pins on the two driver modules, so one acts as a sink whenever the other acts as a source. Consider what happens when WRITE is true, still assuming selection of winding 0. Pin EE is brought to ground and pin EF floats, but the two are connected together, so windings 0 through 7 are connected to ground at one end. In the bottom W108, pin EF is brought to -10V but EE floats. Both outputs are connected to windings 0, 8, 16, ..., but through different sets of diodes, so the floating output has no effect, and the selected windings are brought to -10V at this end. Thus a current of approximately 200 ma flows from the driver in the top W108 through Y-winding 0 to the driver in the bottom W108. Since only one of 15 windings is connected at both ends, there are 14 that are connected at one end but floating at the other and are hence partially selected. Of these, seven are at ground because grounded at the one end, the other seven are at -10V. The 49 remaining Y-windings float.

During read, current flows in the opposite direction because EF in the top W108 is now at -10V, and EE at the bottom is ground while EF floats. The circuits on either side of the stack select a single X-winding in the same manner, with current flowing from right to left during read, from left to right during write.

The combined effect of the read current flowing through the 13 cores at the intersection of the selected X-winding and the selected Y-winding is sufficient to change to 0 any core that is in the 1 state. (It has no effect on those already 0.) Such a state change produces a pulse on the sense winding in the plane that contains the core. The sense windings are connected via the G609 (G608) at the left to the W532 sense amplifiers, contained two per module. These are ac-coupled difference amplifiers with a difference gain of 90 and common mode rejection of 3 to 1. The outputs of each sense amplifier are in turn applied to a G803 ac-coupled rectifying slicer, also contained two per module. If enabled, the strobe produces an output pulse at each slicer that receives a sense signal representing a change from 1 to 0. These output pulses set individual MB bits. If there is no strobe, the net effect of the read is merely to clear the addressed core location.

While write current is flowing, the combined effect on the 13 cores at the intersection of the selected X- and Y-windings is sufficient to change all the cores from 0 to 1 except those in planes that receive inhibit current that acts to oppose the write current. In the upper W108 at the right, the two inhibit levels are applied to both the 0 and 1 inputs of two sets of the decoding diodes, so the drivers are selected entirely by the other eight inputs. Selection is on a negative input, so a given driver supplies inhibit current to prevent the writing of a 1 in any plane that corresponds to an MB bit that is 0. In the lower W108, the inhibit level is applied only to DP and DS and enables those inputs that receive signals from MB or the parity bit PB. The drive select terminals of the W108 are left floating, so the driver outputs switch between ground and -15V. The inhibit windings are connected to the negative driver output terminals and are grounded at the other end so that current flows through the winding into the driver.

The inputs to the lower W108 that receive the read and write levels from memory control are completely isolated from the other inputs, and their drivers act separately as buffers for the signals. The positive outputs are used, but memory control supplies the input levels at ground, so the output is at -15V when the corresponding function is true (when READ is true the read driver is not selected and its positive output is therefore negative). At turn-on the read and write levels must supply 120 ma to the X and Y W108s, 35 ma to each driver at the ground end of a winding, 25 ma to each at the negative end.

3.7 IN-OUT

The IO logic is shown in block schematic 17. IOT instructions use a special sequence that is shown in the flow chart on the lower left-hand side of drawing 29, but IOT events that occur in the main flow are shown in drawing 30. Print 5 shows the signals on the IO bus, with positive and negative pulses shown by open and closed triangles, and levels of the two polarities are shown similarly by diamonds. The signal naming convention has been changed at this point to provide ease of interpretation when dealing with standard PDP-8 options which are used on the PDP-8/S. The inputs from the information

collector listed at the left go directly to AC. The levels from AC and MB listed in the second and third columns are for data output and device selection. The remaining signals are received or generated by the logic shown in print 17.

In the center of that block schematic are a pair of one-shot delays that generate a separate IO pulse train that is parallel to the bit time pulses. In execute time of an IOT, A00 triggers a PA to set the first one-shot, and 1 μs later its transition back to 0 triggers the second one-shot, which also has a period of 1 μs. The IO pulses are derived from the PA output and the 1 outputs of the delays, but they are microprogrammed. Therefore only those called for by the IOT are actually generated. Thus at the lower left a 1 in instruction bit 11 allows the PA output to trigger IOP1. Just above it a 1 in bit 10 produces IOP2 from the output of the first delay. At the top of the drawing the third pulse IOP4 is generated from the second delay if bit 9 is 1.

The gate below the INS flip-flop decodes the device selection portion of an IOT for the code 00, which selects the program interrupt. When PI is selected, IOP1 sets INS; IOP2 clears both it and ION to turn off the interrupt. Setting INS turns on the interrupt by setting ION at the first pulse in the next fetch time. When the interrupt is on, an interrupt signal over the bus or the occurrence of a parity error (upper left) requests a program interrupt by causing A12 to set PIR. An interrupt is also requested by LPC setting as power is failing (C3). Every A13 clears PIR, but the interrupt signal is a level, so every A12 sets it again until the level goes away. When the break is granted, A00 clears both INS and ION to prevent further interruptions.

The other "devices" contained in the processor are the parity and power failure logic. Both are selected by the code 10 which is decoded by the net at the lower right. When this selection is made, IOP1 causes a skip if there is no parity error. IOP2 skips if there is a power failure (i.e., LPC is 1). The output of the parity and power checking nets are ORed with the skip signal from the bus to produce IOSKP, which is gated by IOT at the far left to produce IOSKS, which in turn sets the skip flip-flop (SKP). If IOP4 is programmed, the IOT also clears PE.

The clear pulse shown at the lower right clears all IO equipment only when the start key is pressed and on power clear. A clear AC signal from the bus (upper left corner) produces CAC, the clear pulse for that register.

3.8 TELETYPE

The circuits and bus connections for the teletype control are shown in drawing PT08-A-1. The teletype is actually two separate devices, one for input, the other for output; and all logic for transmission of information between computer and teletype is contained in two modules, a receiver and a transmitter. Since these are separate devices, there are two device selectors: device code 03 selects the receiver, 04 selects the transmitter. The transmitter and receiver also require separate clocks (upper left-hand side of drawing), both set at about 220 Hz (both have periods between 4.5 and 4.6 ms,

but the transmitter clock runs slightly faster than the receiver clock). The transmitter clock is always on, the receiver clock functions only when enabled from the receiver module.

Data transmission between computer and teletype control is in 8-bit characters sent to or taken from AC04-11. AC11 corresponds to the first character bit and the eighth bit (AC04) is always 1. Between the control and the ASR 33, data transmission is in the form of 11-unit characters that are presented serially at 110 bits per second, so one complete character requires 100 ms. Character transmission always begins with a start impulse (space), followed by the eight data bits in order (with 1s represented by marks), and transmission is terminated by a stop impulse (two marks). An idle line marks continuously.

The logic that is internal to the W706 receiver and W707 transmitter modules is shown only in the circuit schematics, and the conventions used are different from those used in the computer block schematics. Here the voltage levels are high and low, where high is defined as any voltage in the range 0.85 to 3.6V, and low is the range of 0 to 0.4V. Voltage dividers at all module inputs and outputs translate the high and low levels to (and from) the computer ground and negative levels. A D-shaped symbol represents an AND gate in which two low inputs produce a high output; the arrow-shaped gate is an OR in which the output is low if either input is high. A circle at any input or output indicates a transition from high to low whenever the circuit function is satisfied, or flip-flop goes to the given state, etc. A flip-flop is defined as being in the 1 state when its 1 output is low. A transition from high to low at the T-input sets the flip-flop if only S is low, clears it if only C is low, but complements it if both are low. The input at the side of a flip-flop has no circle and sets or clears it (whichever the case may be) on a low to high edge.

3.8.1 Input

For the teletype input logic, refer to the circuit schematic of the W706 receiver. The clock input (on the lower left-hand side of the drawing) is the input shown as RCLO on the block schematic. Proceeding clockwise around the circuit schematic, the input at BV is I/O CLEAR, the clear flag input is IOT032, the reader run output is RRE, the flag output is the interrupt signal, the strobed flag output is the skip signal, and the strobe for reading the flag is IOT031. The bit outputs are IC11-04, with bit 8 at the bottom corresponding to IC04. The read strobe for the input shift register is IOT034, and the clock enable output is RCLE.

The serial input from the teletype is at bottom center of the schematic (this is labeled TSO on the block). Whenever a key is struck or a line is read on paper tape, the distributor begins transmission with a space which changes the input from high to low. This enables the receiver clock and the first RCLO sets ACTIVE, whose 0 side transition from high to low sets all bits in the shift register, clears FLAG DLY, and clears READER RUN so that if input is from the reader only a single frame will be read. The 1 state of ACTIVE holds the enabling level to the clock so it will continue throughout the input cycle.

The first clock also sets the frequency divider flip-flop, so that the second pulse, which is centered in the input unit, clears it (see the flow chart in the center of print 29). The low-to-high transition at its 1 output shifts the contents of the register upward and reads the present input into bit 8. Since each input cycle always begins with a space, bit 8 clears. Then each subsequent pair of clocks sets and clears the frequency divider to read another unit of the character into bit 8 and shift up the data that was previously read. At the time the eighth character bit is being read, the 0 resulting from the initial space is in bit 1, so the shift also sets FLAG to request an interrupt, and sets FLAG DLY Once the FLAG DLY flip-flop is set, the next clock sets IN LAST UNIT, and the succeeding one clears ACTIVE and sets STOP 1. Although ACTIVE is now clear, in LAST UNIT holds on the clock enable so the next clock sets STOP 2 and clears STOP 1. With both stop flip-flops set, the final clock clears them both and clears IN LAST UNIT to disable the clock. The final three clocks are not necessary for reception, but they prevent noise on the line from triggering a new input cycle at least for the first one and a half units of the two-unit stop impulse.

The program can determine the source of the interrupt by using an IOT031 to skip on the flag. An IOT that selects teletype input and has 1s in bits 9 and 10 clears AC at IOP2 and loads the character into AC04-11 at IOP4. The inverter through which IOT032 generates the clear signal for AC is shown at the top left-hand side of the schematic for the W707 transmitter module. The same IOT that clears AC also clears FLAG, and sets READER RUN so that another frame will be read if the reader is on.

3.8.2 Output

For the teletype output logic refer to the circuit schematic for the W707 transmitter. The clock input at the lower left is the TCLO input on the block schematic. Proceeding clockwise around the circuit schematic, the power clear input is I/O CLEAR, the clear flag input is IOT042, and the input at BJ is IOT032 which produces the CLR AC pulse at AP. IOT041 strobes the flag and the strobed output causes a skip; the flag output is the interrupt signal and the output line that drives the print selector magnets is labeled PSM on the clock. The data inputs to the shift register are BAC levels 11-04 the last corresponding to bit 8. The pulse that loads the buffer at the bottom right is IOT044, and it always sets ENABLE because pin BS is grounded.

As shown at the top of the output flow chart on the right-hand side of drawing 29, by selectir device code 04 the program can skip on the flag to determine when the transmitter is free, and IOP2 clears the flag. Loading a character into the shift register sets ENABLE, allowing transmission to begin on the next clock provided that the previous transmission is complete. If the program gives the IOT044 while the stop impulse for the previous character is still on the line, the clock continues to transmit that signal and does not begin the new character until both stop flip-flops are set and FLAG DLY is clear.

When transmission does begin the first TCLO sets ACTIVE, which clears LINE to begin transmission with a space. The next clock (which clears STOP 2) sets the frequency divider, so that the

following clock (which clears STOP 1) clears the frequency divider to shift the first bit of the character into LINE for transmission. The shift also clears ENABLE and moves the rest of the character up one bit. Each pair of clocks then alternately sets and clears the frequency divider and moves another bit into LINE for transmission. After the last character bit is transmitted, the next shift moves the 1 originally in ENABLE into LINE to begin transmission of the stop impulse. All bits of the shift register are then clear, so the next clock clears ACTIVE, sets FLAG DLY, and sets FLAG to request an interrupt.

Subsequent clocks then time out the two marks required for the stop, the next clock clearing FLAG DLY and setting STOP 2, and the final one setting STOP 1. A new character can be loaded into the shift register anytime after FLAG is set. After completion of the stop signal, a 1 in ENABLE causes a new transmission cycle to begin. So long as ENABLE is clear, LINE remains set to continue marking the line.

CHAPTER 4
MAINTENANCE

DEC Field Services supplies an up-to-date list of recommended spare parts for the PDP-8/S. The list includes not only module, semiconductor and miscellaneous spares for the computer, but also spares and necessary tools for the teletype. In addition, it is recommended that the user have the following items to maintain the computer and teletype.

Item	Description
Multimeter	Triplett Model 630-NA; Simpson Model 260
Dual-channel oscilloscope	Tektronix 580 series, preferably with delayed sweep trigger facilities
ASR 33 lubricants	Teletype KS7470 oil, KS7471 grease
Lint-free cloths	Cheese cloth or equivalent
Cotton swabs	Q-tips or equivalent
Cleaning fluids	Dupont Freon TF; denatured alcohol
Test cables and probes	Low-capacity probes for the oscilloscope, alligator clips, etc.
Super Filter Kote (aerosol)	Research Products Corp., Madison, Wisconsin

DEC supplies the following manufacturers manuals for lubrication and adjustment procedures and corrective maintenance for the teletype:

Teletype Bulletin 273B:	Model 33 Automatic Send-Receive Teletypewriter Set (ASR), Vols 1 and 2
Teletype Bulletin 1184B	Parts, Model 33 Automatic Send-Receive Teletypewriter Set (ASR)

4.1 MAINTENANCE PROGRAMS

MAINDEC programs permit self-testing of the PDP-8/S for checkout, preventive maintenance, or diagnosing equipment malfunctions. Each MAINDEC package consists of program tapes and a reference document. All documents have the same format, and an outline of this format, as well as the documents and tapes themselves, are available from the DEC PDP-8/S Program Library. In particular, §1 of the document is an abstract of the program; § 3, 4 and 5 give complete details for loading, starting, and running the program, §6 § 10 and 11 contain flow charts and the program listing.

The MAINDECs listed below are applicable to the PDP-8/S processor, memory and teletype. In a number of a tape, PB following the slash indicates a paper tape in binary format, PM indicates a paper tape in readin mode format.

	Document No.	Tape No.
Basic Instruction Test	801-1/D	801-1/PM
Instruction Test 1	8S-D01A/D	8S-D01A/PB
Instruction Test 2	8S-D02A/D	8S-D02A/PB
Instruction Test Part 2B	801-2B/D	801-2B/PB
Basic JMP-JMS Test	8S-D03A/D	8S-D03A/PB
Random JMP Test	8S-D04A/D	8S-D04A/PB
Random JMP-JMS Test	8S-D05A/D	8S-D05A/PB
Random DCA Test	8S-D06A/D	8S-D06A/PB
Random ISZ Test	8S-D07A/D	8S-D07A/PB
Memory Checkerboard (two tapes - low and high)	802/D	802/PM
4K Memory Address Test	8S-D11A/D	
Low		8S-D11A/PB 8S-D11A/PM
High		8S-D11J/PB 8S-D11J/PM
4K Sense Amplifier Test	8S-D15A/D	8S-D15A/PB
Extended Memory Control	820-1/D	820-1/PB(?)
Extended Memory Checkerboard	820-2/D	820-2/PB(?)
Memory Power On/Off Test	829/D	829/PB
Teletype Reader Test	810/D	810/PM
Teletype Reader Exerciser	810A/D	810A/PM
Teletype Punch Test	812/D	812/PM
Teleprinter Test	814/D	814/PM

4.2 MEMORY ALIGNMENT

The memory is a very simple coincident current system with only two adjustments. The master current adjustment is the pot on the A702 reference supply. The strobe adjustment is through the R401 located in 1E22 (8K) or 1F36 (4K). Adjusting the clock affects both the width and position of the strobe simultaneously. Note that it also affects total memory cycle time as well as the read, write and inhibit times.

The memory is aligned during the heat test in checkout. Unless the clock and reference supply pots are jarred severely in transit, they should be aligned properly when received. The reference supply voltage is easily measured at the tabs on the handle end of a W108 or G609 (G608 in 4K). This voltage varies with temperature and best tuning is achieved at 130°F, because at this upper spec temperature the shmoo characteristic has a much smaller area. With the machine stabilized at normal room temperature (68°F), the stack operating temperature will be on the order of 73°F.

The temperature compensation thermistor is located on the rear memory stack module. The thermistor on the front module is a spare. Compensation is not linear and causes the tab voltage to move toward zero when the temperature is increased. Nominal voltages are as follows.

	Ambient	0°C 32°F	25°C 77°F	54.5C 130°F
Stack				
~~Ferroxcube~~		-13.3V	-11.9V	-9.4V
EMI		-13.1V	-11.6V	-9.0V

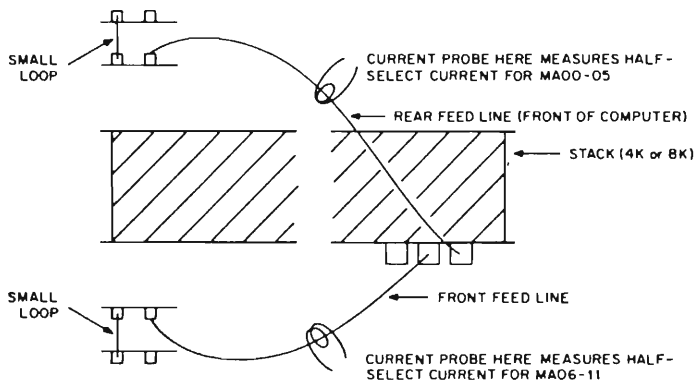
The best place to measure memory timing is the MEMGO signal at 1D36N. The negative level found here represents the memory cycle time, which is nominally ~~6.3 μs for a Ferroxcube stack,~~ 6.5 μs for an EMI stack*. The value may vary from stack to stack by about 100 ns as it is set by averaging the upper and lower failure points while the machine is in heat. At room temperature, the setting may not necessarily be the average of the room temperature upper and lower failure points, but this is proper as the shmoo of either stack expands in area as the temperature drops.

In any case, the 1 output for any bit measured at the output of a W532 sense amp should be 2V peak (4V peak-to-peak).

4.3 MEMORY TROUBLESHOOTING

4.3.1 X-Y Selection

Failure to select a particular block of locations or even single locations in some fixed pattern of blocks in core generally indicates a bad W108 selection driver. By using a current probe, it is very simple to check all selection drivers with a small program loop. First, rearrange the tab wiring on the handle end of the W108s so that the current regulator on the front stack module is driving the front and rear W108 pairs in parallel.

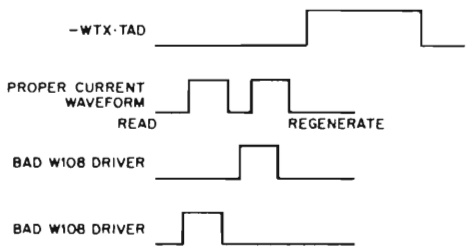


*Room temperature, R401 period coefficient is -0.15% 1°C.

Without using locations 0-7, 10, 20, 30, 40, 50, 60, 70, 100, 200, 300, 400, 500, 600, 700, 1000, 2000, 3000, 4000, 5000, 6000, 7000, put this loop in some area of core that works.

```
        LAS
        DCA .+3
        TAD I .+2
        JMP .-3
0
```

Start the program and place the current probe on the front feed line. Sync scope negative on WTX ·TAD (1A18D) and look at -WTX -TAD (1A18E) with the other scope trace. -WTX ·TAD is a positive waveform. Just prior to its rising edge is a current waveform that represents the address selected by any combination of MA06-11. Run the loop through the 16 combinations, 0-7, 10, 20, 30, 40, 50, 60, 70, on the SR switches. If a driver is failing, a missing current pulse will be observed as shown below.



The W108 can be localized by moving the current probe to the small loop between adjacent waveforms once the bad address combination is found.

Move the current probe to the rear feed line, and repeat the above procedure using addresses on the SR switches of: 100, 200, 300, 400, 500, 600, 700, 1000, 2000, 3000, 4000, 5000, 6000, 7000. This simple procedure checks all drivers in the selection system.

4.3.2 Inhibit Drivers

Place this loop (if runable) in core.

```
        LAS
        DCA .+2
        JMP .-2
```

Set the switch register to all 1s and place a current probe on the feed line from the rear stack module to the first W108 inhibit driver. Sync on WTX ·DCA (1B08R) and observe -WTX ·DCA)1B08S). Turn off

one switch (put a 0 in one bit in the SR word). The current waveform appearing just prior to the negative-going edge of -WTX ·DCA is the inhibit current for the bit selected by the switch.

4.3.3 Sense Amplifiers and Slicers

Problems in these circuits generally are accompanied by a parity error indication on the front panel. The first thing to check for is an error that seems to be intermittent and/or is very sensitive to temperature changes.

The following simple loop, which writes the SR switches everywhere in core except where the program resides and allows parity errors to interrupt, is very helpful in tracking a dropout or pickup problem.

Location	Instruction Octal	Mnemonic	Definition
1	6104	CMP	/Clear PE on parity error /only
2	7200	CLA	
3	5010	JMP 10	
10	6001	ION	/Enable interrupt
11	1022	TAD 22	/Set location counter
12	3023	DCA 23	
13	7604	LAS	/Read pattern from SR
14	3423	DCA I 23	/Store
15	1423	TAD I 23	/Retrieve
16	2023	ISZ 23	/Index counter
17	5013	JMP 13	/Repeat
20	7200	CLA	/Finished, start again
21	5011	JMP 11	
22	0024		
23	0		

The program writes SR in locations 24 through 7777, and reads each location immediately after writing it. A parity error is most likely to occur as a test location is read, i.e., at the TAD in location 15.

Sync scope negative on PE (1E06T). Observe -PE (1E06S). Positive pulses appearing on this train are parity errors. An error occurs on the memory cycle just before the positive-going edge of -PE. Look at -WTX ·TAD. The error is occurring here if -PE goes positive approximately 6 μs before the positive-going edge of -WTX ·TAD.

A parity error can occur only in data that is read from memory by the processor. By varying the pattern in SR, one may find combinations that increase the frequency of errors. Once the bit has been localized, watch the sense amplifier and slicer behavior just prior to an error. Note that a parasitic oscillation is extremely difficult to observe. Any added capacitance (such as a scope probe) can cure the problem and should be a hint that it is a parasitic.

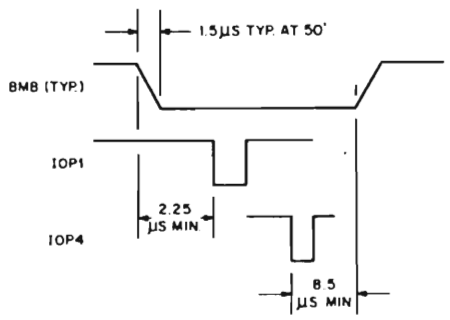
There are two test points on the G803 that are not shown on the logic drawing. These are pin L for inputs J and K and pin S for inputs P and R. The pulse observed here is the slicer action and it shows where slicing begins and ends. Observing the read strobe simultaneously at pin V of any slicer (G803) will aid in adjusting the strobe (memory timing). The strobe should be approximately centered in the slicer test point signal.

4.4 IN-OUT BUS SPECIFICATIONS

The maximum length of the bus including the teletype lines is 50 ft of 92 Ohm coaxial cable. The cables have nine conductors and are fitted with W011 connectors that can be plugged into standard Flip Chip module receptacles. Terminations are required only on the IOP lines, which originate in the computer at B39 pins K, M, and P. A cable terminator (G701) with D664 diodes to ground must be plugged into the spare bus slot in the last device on the bus. The diodes limit overshoot to +0.75V maximum and -0.75V minimum. A G701 terminator is installed in the teletype logic as shipped from DEC. If the teletype is always the last device on the bus, the terminator can be left where it is.

Signals on the bus are as follows.

BMB00-08	Output levels that specify the device address in an IOT. Six pairs of lines represent both 0 and 1 at both 0V and -3V.
Recommended peripheral decoder	W103 with appropriate diodes clipped out
Alternate peripheral decoder	R111 diode gate
Drive available	18 ma maximum at 0V -4.25 ma maximum at -3V
Timing	BMB lines should be used only for strobing by an IOP. They have settled down by BT11 of WTF in the IOT, and they remain static until BT0 of WTE in the IOT. There should thus be no need to worry about slow fall times.
	Typical overshoot on positive-going BMB lines is +2.5V for 200 ns. Overshoots do not affect recommended DEC module types.



BAC00-11

Output levels that supply the contents of AC as data

0V = 1
-3V = 0

Recommended inputs

Level inputs of DCD gates such as in the R203

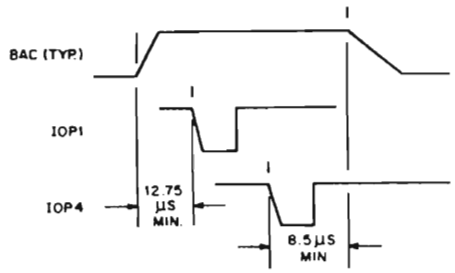
Alternate inputs

R series gates such as R107

Drive available

18 ma maximum at 0V
-8 ma maximum at -3V

Timing



BAC lines can be set up any time prior to an IOT. The shortest time from set up to the earliest IOP is at BT11 of WTE in a TAD. The earliest possible time that BAC lines can change after the latest IOP is at BT12 of WTF in an OPR. Poor fall times on BAC lines need never concern the designer since there is such a large amount of time available prior to the earliest IOP.

Typical overshoot on positive-going BAC lines is +2.5V for 200 ns. Overshoots do not affect recommended DEC module types

IC00-11

Positive input pulses (-3V to ground) that set individual AC bits

Recommended sources

Pulsed outputs, clamped or unclamped, such as R603, R123

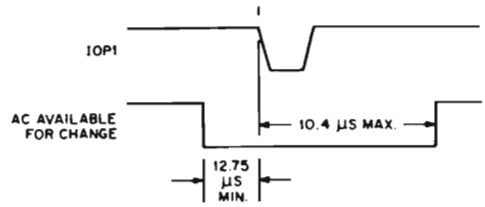
Loading

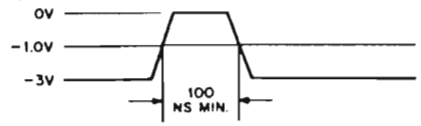
11 ma at 0V in the 8/S
0 ma at -3V in the 8/S

Caution should be exercised when connecting loaded gates to the IC lines as they increase the total drive requirement at 0V.

Timing

Pulses presented to IC lines should originate from an IOP. The maximum time that AC is available for external setting is until the earliest time that AC can be used in the instruction following the IOT. This is BT0 of WTF in an OPR.





The minimum acceptable pulse at the input to the 8/S is as shown here. It is recommended that nominal 400-ns pulses be used at the driving end.

SKIP

Positive input pulse (-3V to ground) that sets the skip control flip-flop from a peripheral device during an IOT.

Recommended sources

Pulsed outputs, clamped or unclamped, such as R603, R123

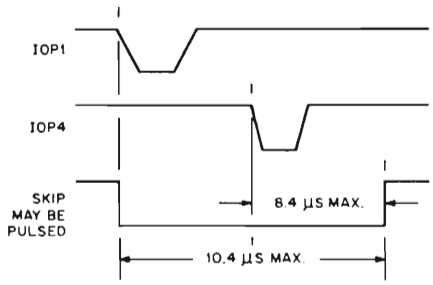
Loading

11 ma at 0V in the 8/S
0 ma at -3V in the 8/S

Caution should be exercised when connecting loaded gates to the skip bus. The total external loading on the bus must not exceed 9 ma.

Timing

Pulses presented to the skip bus should originate from an IOP. The maximum time during which the bus can be pulsed is shown here. The minimum acceptable pulse at the input to the 8/S is the same as shown for IC.



CLEAR AC

Positive input pulse (-3V to ground) that clears AC prior to pulsing the IC lines.

Recommendes sources

Pulsed outputs, clamped or unclamped, such as R603, R123

Loading

20 ma at 0V in the 8/S
0 ma at -3V in the 8/S

External loaded gates cannot be connected to the bus.

Timing

Pulses presented to the clear AC bus should originate from an IOP. The maximum time during which the bus can be pulsed is the same as shown for the skip bus. The minimum acceptable pulse at the input to the 8/S is the same as shown for IC.

I/O CLEAR

Negative output pulses (ground to -3V) that occur when the start key is pressed and when power is turning off or on. The latter two cases generate a burst of pulses.

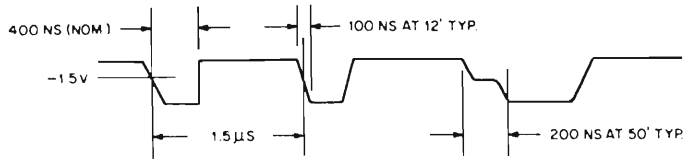
Recommended loads

R107 inverters. If true pulsed lines are required, the PA (R603) pulse input should be driven from an inverter as the rise time of the clear bus pulses cannot be guaranteed less than 60 ns.

Drive available

18 ma maximum at 0V
-1.25 ma maximum at -3V

Timing



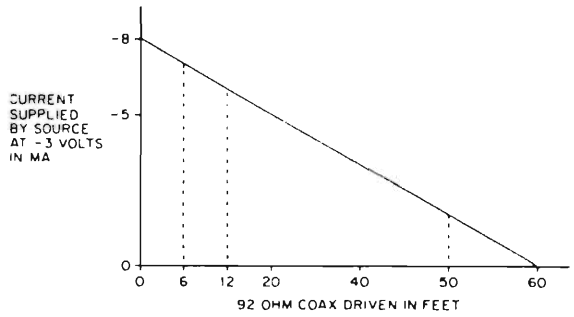
IOP 1, 2,4

Negative output pulses (ground to -3V) that are the primary source of input-output timing for activating and transferring data to and from peripheral devices.

Recommended loads

W103 pulsed inverter inputs R111, R107, etc.

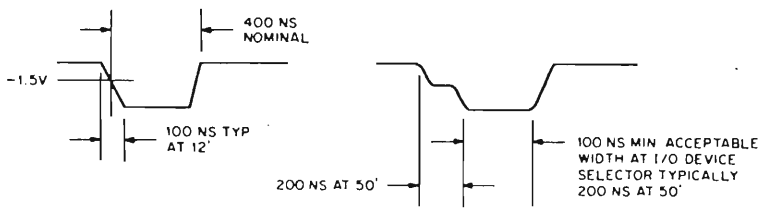
Drive available



72 ma maximum at 0V
-1.25 ma maximum at -3V

The current the IOP lines can supply back into the source at -3V is a function of cable length and a fall time limited to a maximum of 300 ns as shown here.

Timing



INTERRUPT

Level input that causes the computer to interrupt the current program if interrupt synchronization is internally enabled. Bringing the line to ground requests the interrupt; the line is quiescent at -3V.

Recommended inputs

R111, R123, R107, loaded or unloaded

Loading

13 ma at 0V
0 ma at -3V

External loads added must not exceed a total of 7 ma.

Timing

The interrupt line is examined at BT12 of WTE in every instruction. The longest possible time the device must wait for an interrupt request to be recognized is 90 μs.

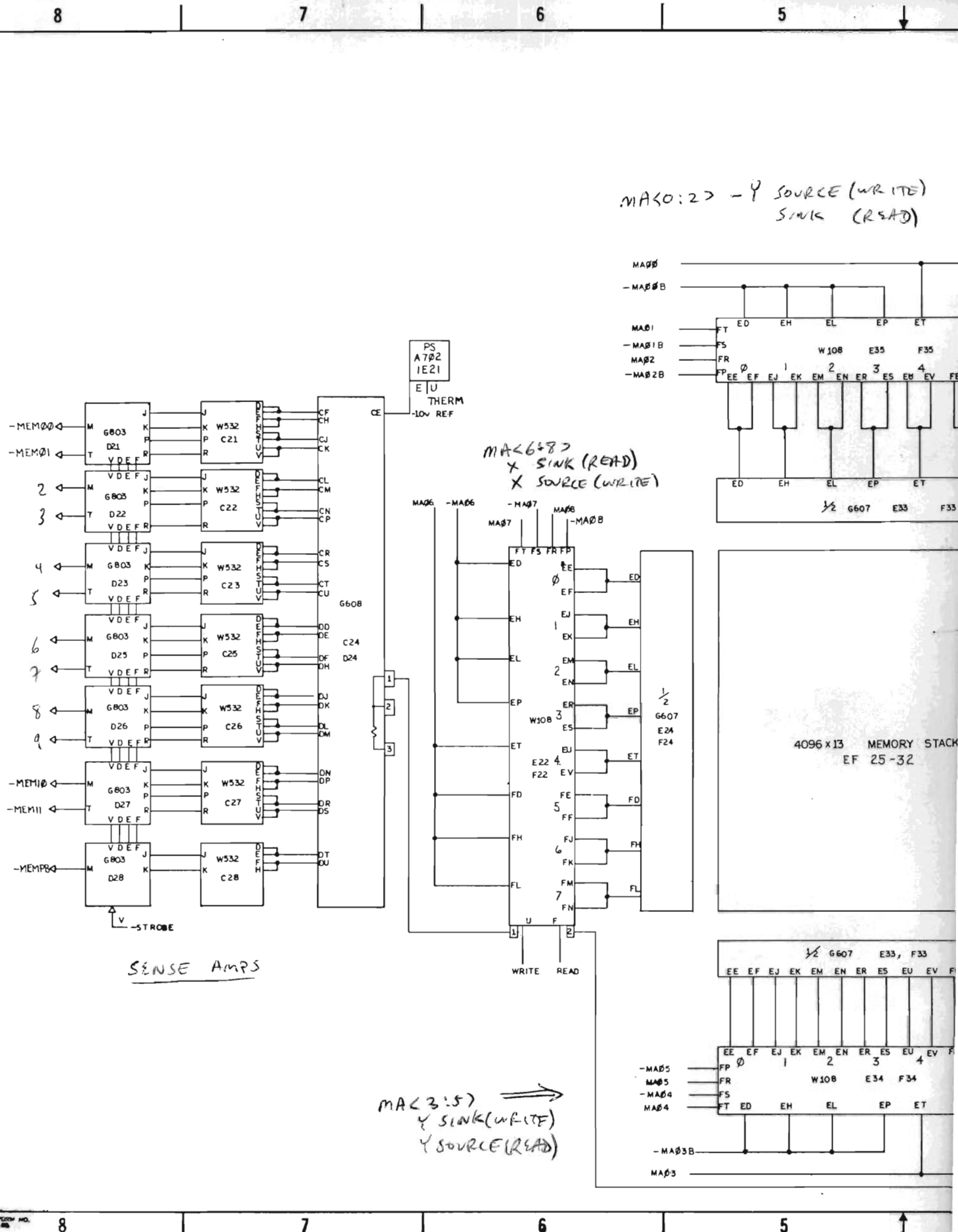
APPENDIX
ENGINEERING DRAWINGS

Reduced copies of the flow charts, logic drawings and circuit schematics are included at the back of this manual. Chapter 3 explains the drawing numbers and the type codes that identify engineering drawings for the PDP-8/S and details the notation and conventions used in the block schematics and flow charts, which are the basis for learning and maintaining the equipment. There are many other engineering drawings, however, used primarily for reference in maintenance.

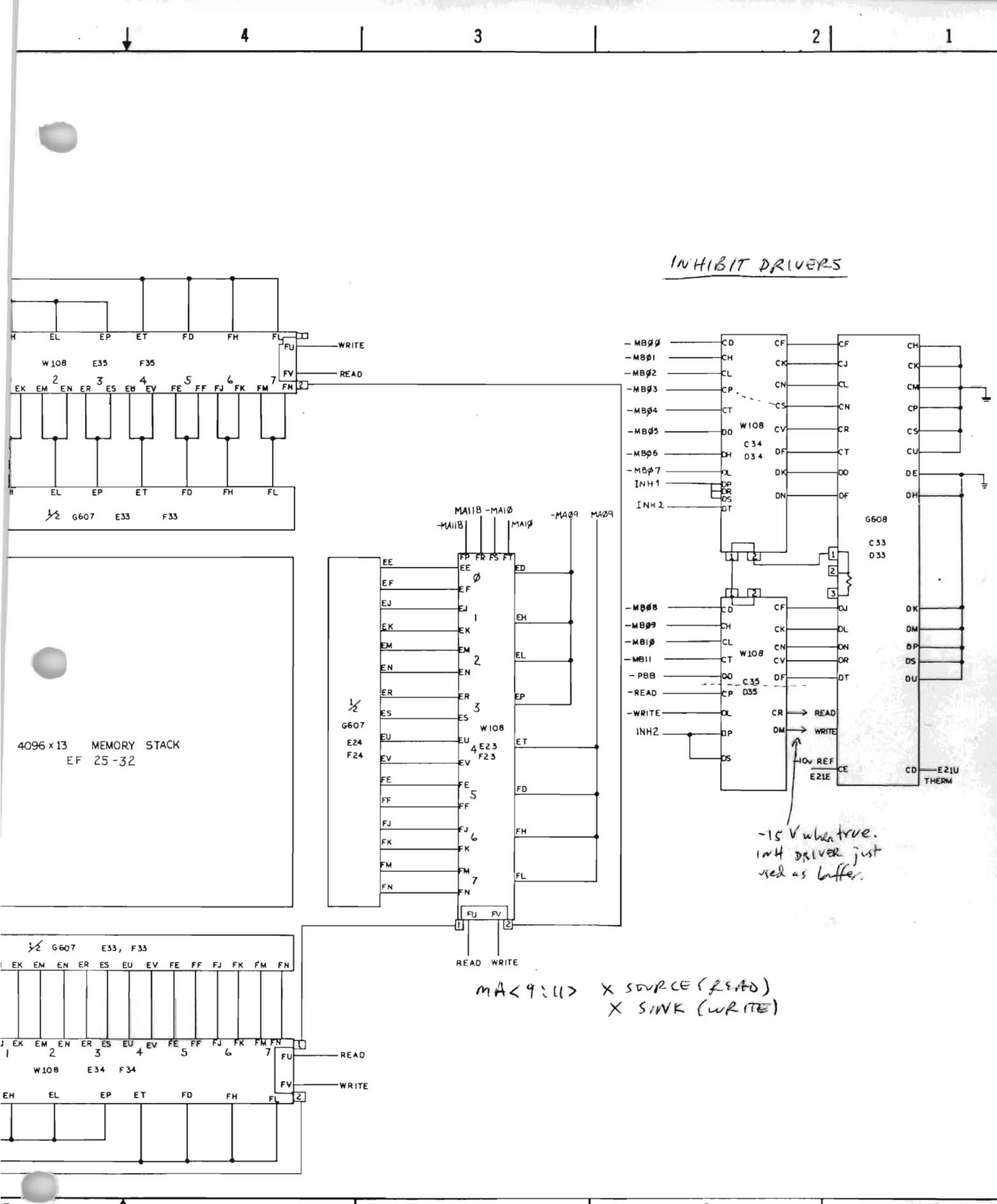
The master drawing list, A-ML-8S-0, lists the block schematics, flow charts, parts list, module utilization drawings, some assembly drawings, and the drawing index list for the computer. This last drawing, D-DI-8S-0-27, lists all mechanical and electrical drawings for the PDP-8/S including the teletype (sheet 2). Sheet 1 is a map showing the relationship among the various categories of drawings.

Detailed information about the modules that make up the processor and memory is given in the module utilization drawings, D-MU-8S-0-25 for the 8K and D-MU-8S-0-26 for the 4K. Each has two sheets showing the six mounting panels, each panel being divided into 40 sections representing the plugin locations. Above the locations are the type numbers of the modules occupying them. Each location is further partitioned according to the individual circuits (flip-flops, pulse amplifiers, inverters) in the module. Circuits are identified by logical function, using the same signal names that appear on the block schematics. For example, a pulse amplifier is labeled by naming the output pulse; an inverter or diode gate is labeled by the output of the net in which it is used. Clamped loads are identified only by the pins to which they are connected.

The rack mounted model uses a standard 728 power supply and 832 power control, which are shown in the circuit schematics. The power supply, circuit breakers, and ac wiring for the table model are shown in the rear panel assembly drawing, D-AD-7005193-0-0.



BS-85-0-4
MEM BLOCK DIAG
(4K)


INHIBIT DRIVERS
4096 x 13 MEMORY STACK
EF 25-32
W108
E35
F35
WRITE
READ
½ G607 E33 F33
MA11B -MAIØ
-MA11B MAIØ
-MAØ9 MAØ9
½ G607 E24 F24
W108
E23 F23
READ WRITE
-MBØØ
-MBØ1
-MBØ2
-MBØ3
-MBØ4
-MBØ5
-MBØ6
-MBØ7
INH1
INH2
W108 C34 D34
G608 C33 D33
-MBØ8
-MBØ9
-MBIØ
-MB11
-PBB
-READ
-WRITE
INH2
W108 C35 D35
READ
WRITE
10V REF E21E
CD E21U THERM
-15V when true.
INH DRIVER just used as buffer.
½ G607 E33, F33
W108 E34 F34
READ
WRITE
MA<9:11> X SOURCE (READ)
X SINK (WRITE)

E38

NAME	FROM	PIN	MODULE TYPE/LOAD	ASS.
		A		
		B		
GND		C		
ICØØ	E3D	D	R001/11MA	◇
ICØ1	E3F	E	R001/11MA	◇
GND		F		
ICØ2	E3J	H	R001/11MA	◇
GND		J		
ICØ3	E3L	K	R001/11MA	◇
GND		L		
ICØ4	E3N	M	R001/11MA	◇
GND		N		
ICØ5	A3T	P	R001/11MA	◇
GND		R		
ICØ6	A3R	S	R001/11MA	◇
ICØ7	A3N	T	R001/11MA	◇
GND		U		
ICØ8	A3L	V	R001/11MA	◇

E37

NAME	FROM	PIN	MODULE TYPE/LOAD	ASS.
		A		
		B		
GND		C		
ICØ9	A3J	D	R001/11MA	◇
ICIØ	A3F	E	R001/11MA	◇
GND		F		
ICII	A3D	H	R001/11MA	◇
GND		J		
SKP	A9K	K	R107/11MA	◇
GND		L		
INT	A40E	M	R107/11MA	◇
GND		N		
CLRAC	A19R	P	R202/20MA	◇
GND		R		
B RUN (1)	B36P	S	R113/18MA	◆
BPAR (1)	F36V	T	R113/18MA	◇
GND		U		
-LCIF	1C31V	V	R282	

BACnn AC output
BMBnn MB output
BMB<3:8> = device#

ICnn input lines (ORs into AC)
SKP skip request
INT interrupt request
CLRAC clear AC
B RUN (1) machine running
BPAR (1) parity bit (goes with BMB)
-LCIF Doesn't actually exist
BIO CLEAR clear all devices
IOPn IOT instruction pulses

these to respond to IOT instructions.

◆ true low
◇ true ground
▷ positive pulse
▶ negative pulse

CL-85-0-5
BUS SCHED

MODULE TYPE/LOAD	ASS.
R001/11MA	→
R001/11MA	→
R001/11MA	→
R001/11MA	→
R001/11MA	→
R001/11MA	→
R001/11MA	→
R001/11MA	→

E39

NAME	FROM	PIN	MODULE TYPE/LOAD	ASS.
		A		
		B		
GND		C		
BAC 0(1)	D5F	D	R107/18ma	◇
BAC 1(1)	D5J	E	R107/18ma	◇
GND		F		
BAC 2(1)	D5L	H	R107/18ma	◇
GND		J		
BAC 3(1)	D5N	K	R107/18ma	◇
GND		L		
BAC 4(1)	D5R	M	R107/18ma	◇
GND		N		
BAC 5(1)	D5T	P	R107/18ma	◇
GND		R		
BAC 6(1)	C5F	S	R107/18ma	◇
BAC 7(1)	C5J	T	R107/18ma	◇
GND		U		
BAC 8(1)	C5L	V	R107/18ma	◇

E40

NAME	FROM	PIN	MODULE TYPE/LOAD	ASS.
		A		
		B		
GND		C		
BMBØØ(Ø)	C36D	D	R107/18MA	●
BMBØ1(Ø)	C36F	E	R107/18MA	●
GND		F		
BMBØ2(Ø)	C36J	M	R107/18MA	●
GND		J		
BMBØ3(1)	B37F	K	R107/18ma	●
GND		L		
BMBØ3(0)	B37J	M	R107/18ma	●
GND		N		
BMBØ4(1)	B37L	P	R107/18ma	●
GND		R		
BMBØ4(0)	B37N	S	R107/18ma	●
BMBØ5(1)	B37R	TT	R107/18ma	●
GND		U		
BMBØ5(0)	B37T	V	R107/18ma	●

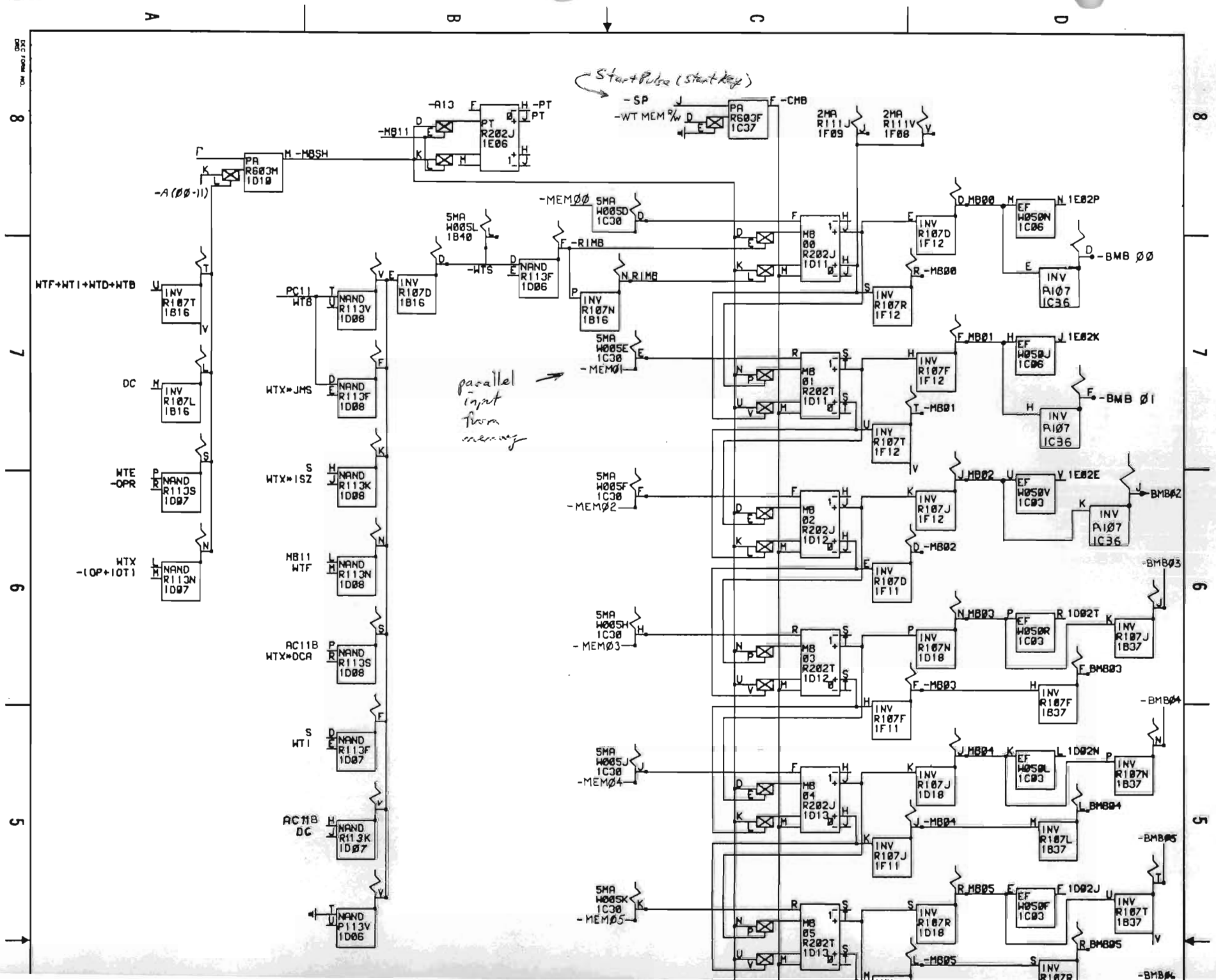
MODULE TYPE/LOAD	ASS.
R001/11MA	→
R001/11MA	→
R001/11MA	→
R107/11MA	→
R107/11MA	◇
R202/20MA	→
R113/18MA	●
R113/18MA	◇
R282	

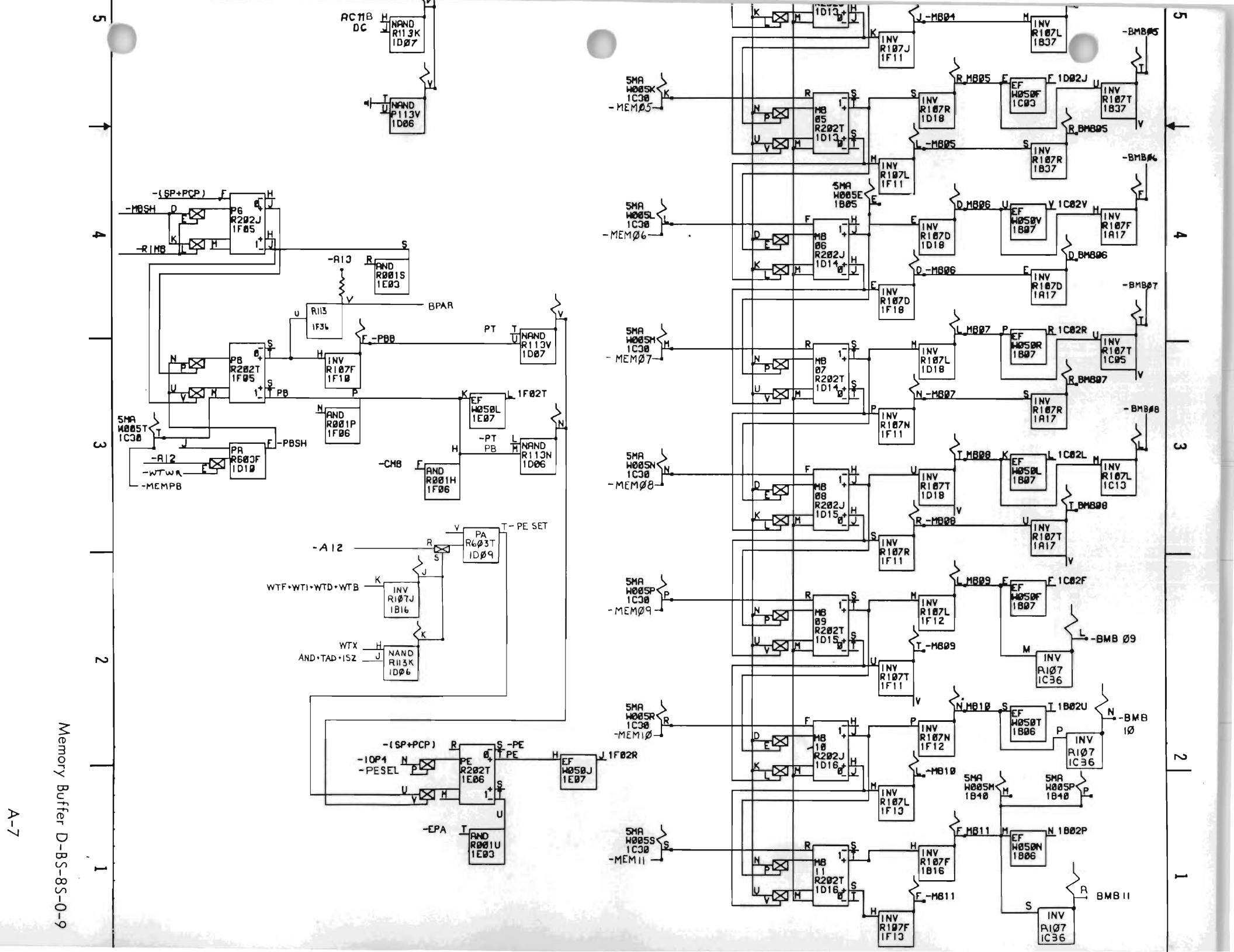
B39

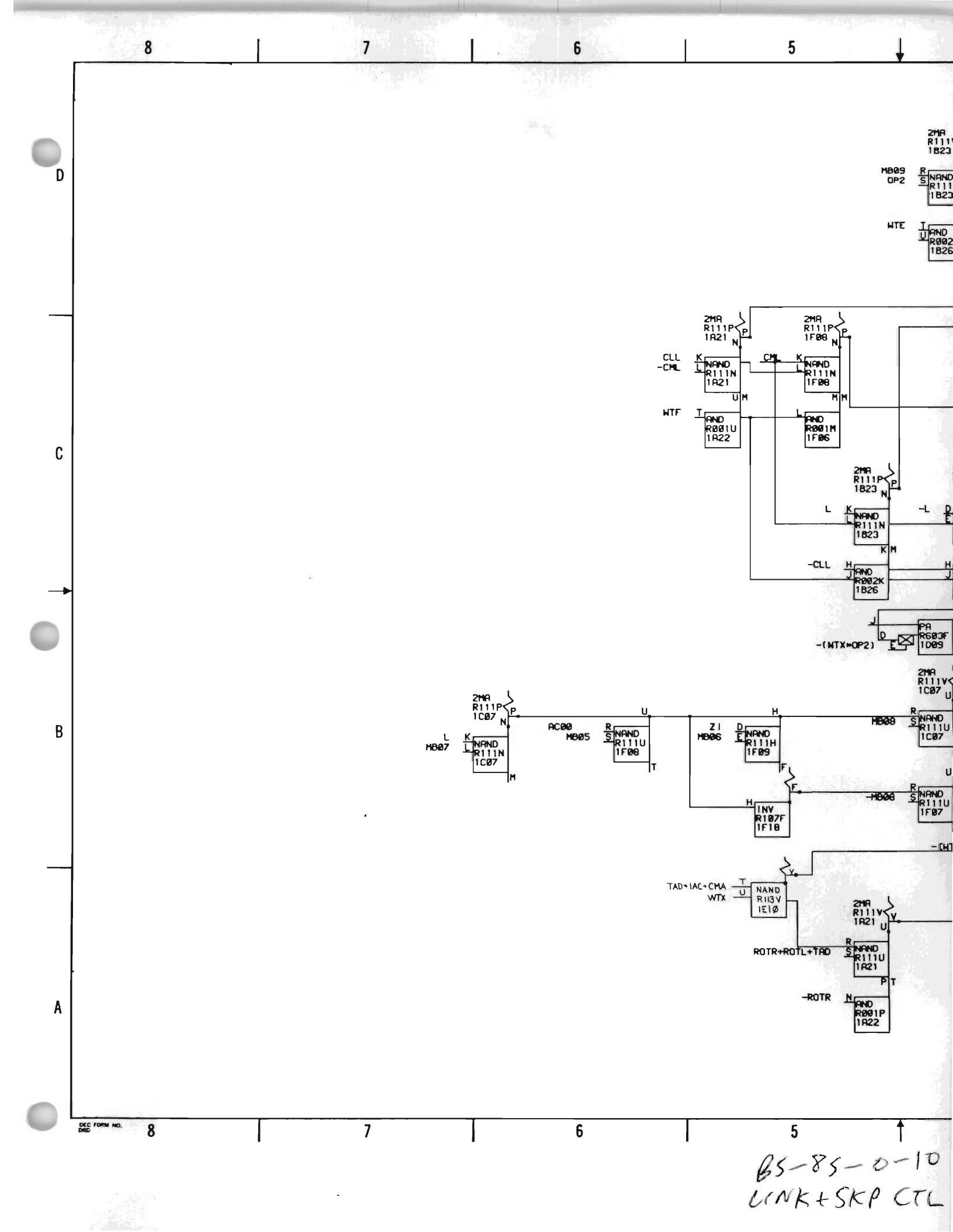
NAME	FROM	PIN	MODULE TYPE/LOAD	ASS.
		A		
		B		
GND		C		
BAC 9(1)	C5N	D	R107/18ma	◇
BAC 10(1)	C5R	E	R107/18ma	◇
GND		F		
BAC 11(1)	C5D	H	R107/18ma	◇
GND		J		
IOP1	A40J	K	4-R107/72MA	→
GND		L		
IOP2	A40M	M	4-R107/72MA	→
GND		N		
IOP4	IB37Ø	P	4-R107/72MA	→
GND		R		
		S		
		T		
GND		U		
B I/O CLEAR	A17L	V	4-R107/72MA	→

D40

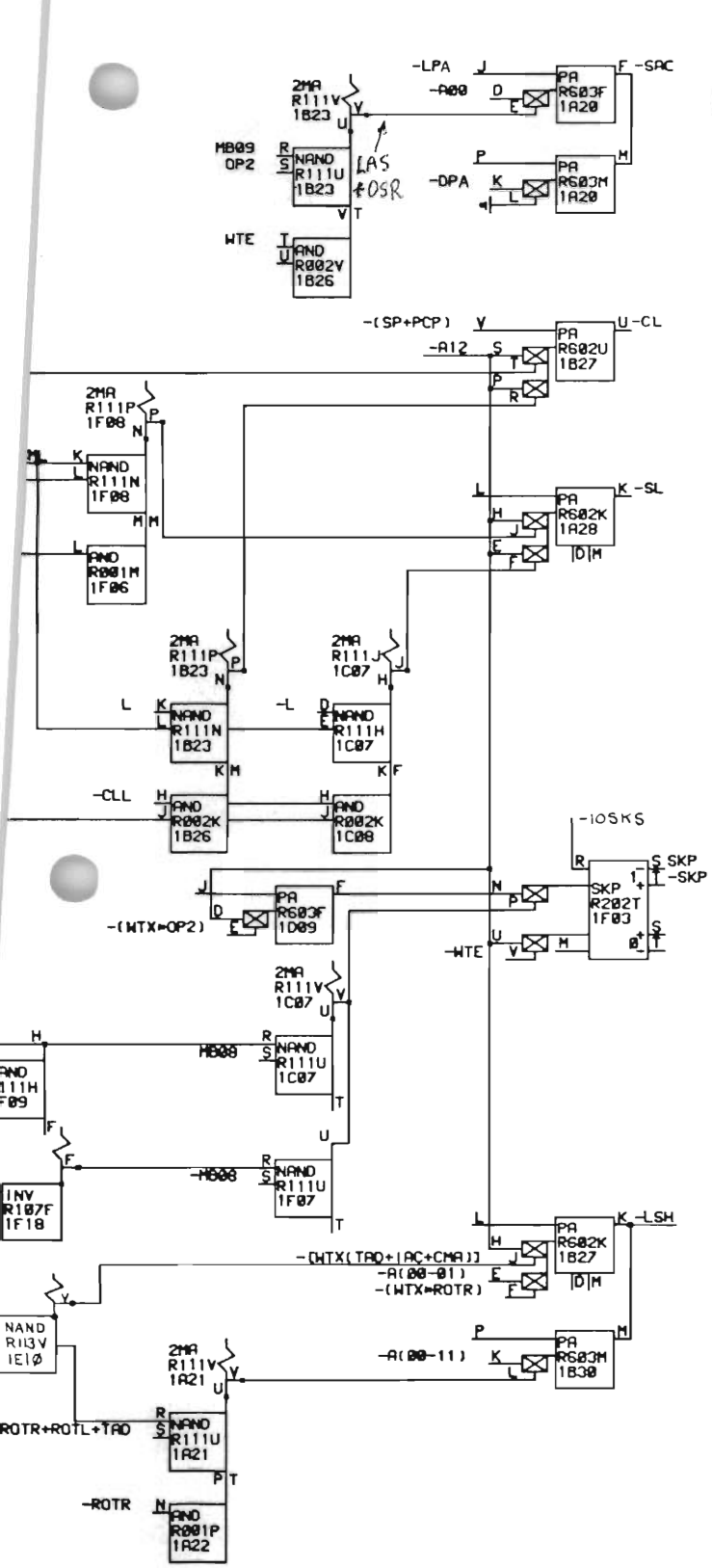
NAME	FROM	PIN	MODULE TYPE/LOAD	ASS.
		A		
		B		
GND		C		
BMBØ6(1)	A17D	D	R107/18ma	●
BMBØ6(0)	A17F	E	R107/18ma	●
GND		F		
BMBØ7(1)	A17R	H	R107/18ma	●
GND		J		
BMBØ7(0)	C05T	K	R107/18ma	●
GND		L		
BMBØ8(1)	A17T	M	R107/18ma	●
GND		N		
BMBØ8(0)	C13L	P	R107/18ma	●
GND		R		
BMBØ9(Ø)	C38L	S	R107/18MA	●
BMB 1Ø(Ø)	C36N	T	R107/18MA	●
GND		U		
BMB 11(Ø)	C36R	V	R107/18MA	●


Start Pulse (Start Key)
-SP
-WT MEM P/W
-CMB
-A13
-MB11
-MBSH
-A(ØØ-11)
-MEMØØ
-MEMØ1
-MEMØ2
-MEMØ3
-MEMØ4
-MEMØ5
-RIMB
-WTS
parallel input from memory
WTF+WT1+WTD+WTB
DC
WTE -OPR
WTX -(OP+IOT1
PC11 WTB
WTX»JMS
WTX»ISZ
MB11 WTF
AC11B WTX»DCA
WT1
AC11B DC
-BMB ØØ
-BMB Ø1
-BMBØ2
-BMBØ3
-BMBØ4
-BMBØ5
BS-85-0-9
Main BFR

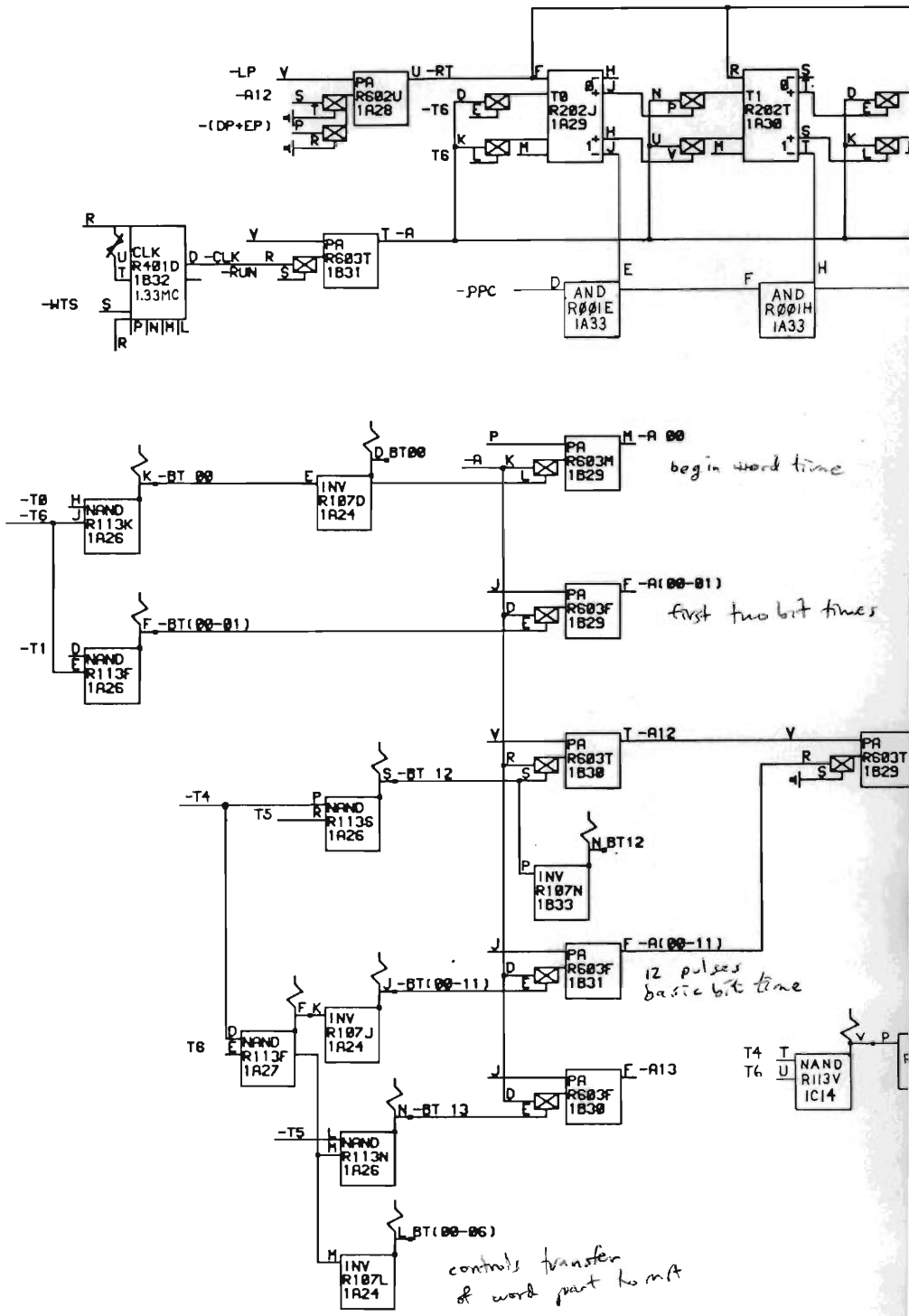

AC11B DC
NAND R113K 1D07
NAND P113V 1D06
-(SP+PCP)
-MBSH
-RIMB
PG R202J 1F05
-A13
AND R001S 1E03
BPAR
R113 1F36
PB R202T 1F05
-PBB
INV R107F 1F10
PT
NAND R113V 1D07
PB
EF W050L 1E07
1F02T
AND R001P 1F06
5MA W005T 1C30
PA R603F 1D10
-PBSH
-A12
-WTWR
-MEMPB
-PT PB
NAND R113N 1D06
-CMB
AND R001H 1F06
PA R603T 1D09
T-PE SET
WTF•WTI•WTD•WTB
INV R107J 1B16
WTX AND•TAD•ISZ
NAND R113K 1D06
-(SP+PCP)
-IOP1 -PESEL
PE R202T 1E06
-PE PE
EF W050J 1E07
1F02R
-EPA
AND R001U 1E03
5MA W005K 1C30
-MEM05
MB 05 R202T 1D13
INV R107J 1F11
INV R107L 1B37
-BMB05
INV R107R 1D18
EF W050F 1C03
1D02J
INV R107T 1B37
INV R107L 1F11
5MA W005L 1C30
-MEM06
MB 06 R202J 1D14
INV R107D 1D18
EF W050V 1B07
1C02V
INV R107F 1A17
INV R107D 1F18
INV R107D 1A17
-BMB06
5MA W005M 1C30
-MEM07
MB 07 R202T 1D14
INV R107L 1D18
EF W050R 1B07
1C02R
INV R107T 1C05
INV R107N 1F11
INV R107R 1A17
-BMB07
5MA W005N 1C30
-MEM08
MB 08 R202J 1D15
INV R107T 1D18
EF W050L 1B07
1C02L
INV R107L 1C13
INV R107R 1F11
INV R107T 1A17
-BMB08
5MA W005P 1C30
-MEM09
MB 09 R202T 1D15
INV R107L 1F12
EF W050F 1B07
1C02F
INV R107T 1F11
INV R107 1C36
-BMB 09
5MA W005R 1C30
-MEM10
MB 10 R202J 1D16
INV R107N 1F12
EF W050T 1B06
1B02U
INV R107 1C36
-BMB 10
INV R107L 1F13
5MA W005M 1B40
5MA W005P 1B40
5MA W005S 1C30
-MEM11
MB 11 R202T 1D16
INV R107F 1B16
EF W050N 1B06
1B02P
INV R107F 1F13
BMB11
INV R107 1C36



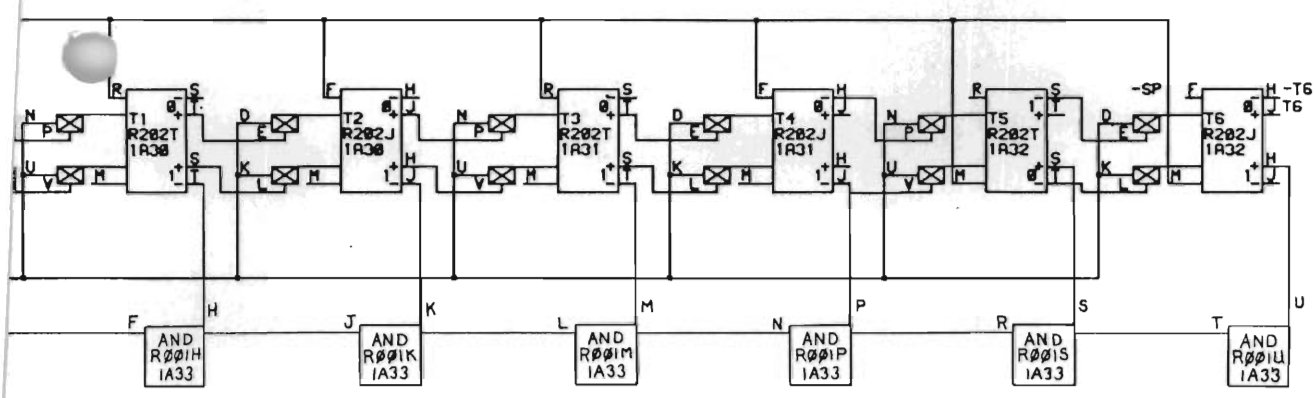
BS-85-0-10
LINK+SKP CTL



passes through switches to AC set inputs.



BS-85-0-11
BIT TIMING



-A ØØ

-A(ØØ-Ø1)

PPC + LP + DP + EP ØØØØØØ1

SP A ØØØØØØØ A13

A 1ØØØØØØ AØØ
A 11ØØØØØ
A 111ØØØØ
A 1111ØØØ
A 11111ØØ
A 111111Ø
A 1111111
A Ø111111
A ØØ11111
A ØØØ1111
A ØØØØ1 11
A ØØØØØ11

A ØØØØØØ1 A12

A(ØØ-11)

-A12 V PA R603T 1B29 -A(ØØ-12)

R S

12 pulses basic bit proc + 1 for carry

T12

-A(ØØ-11)

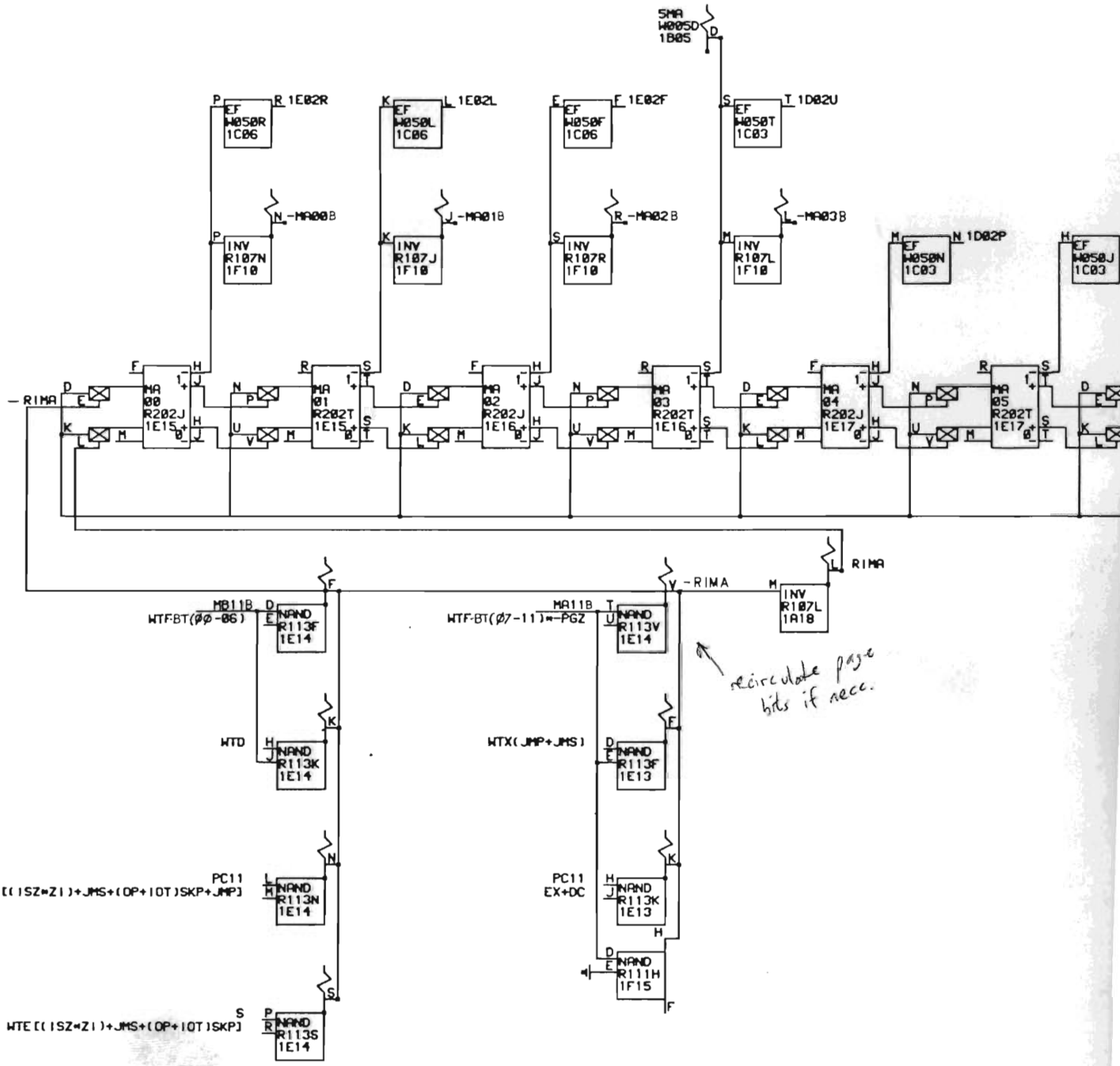
-A13

T4 T T6 U NAND R113V 1C14

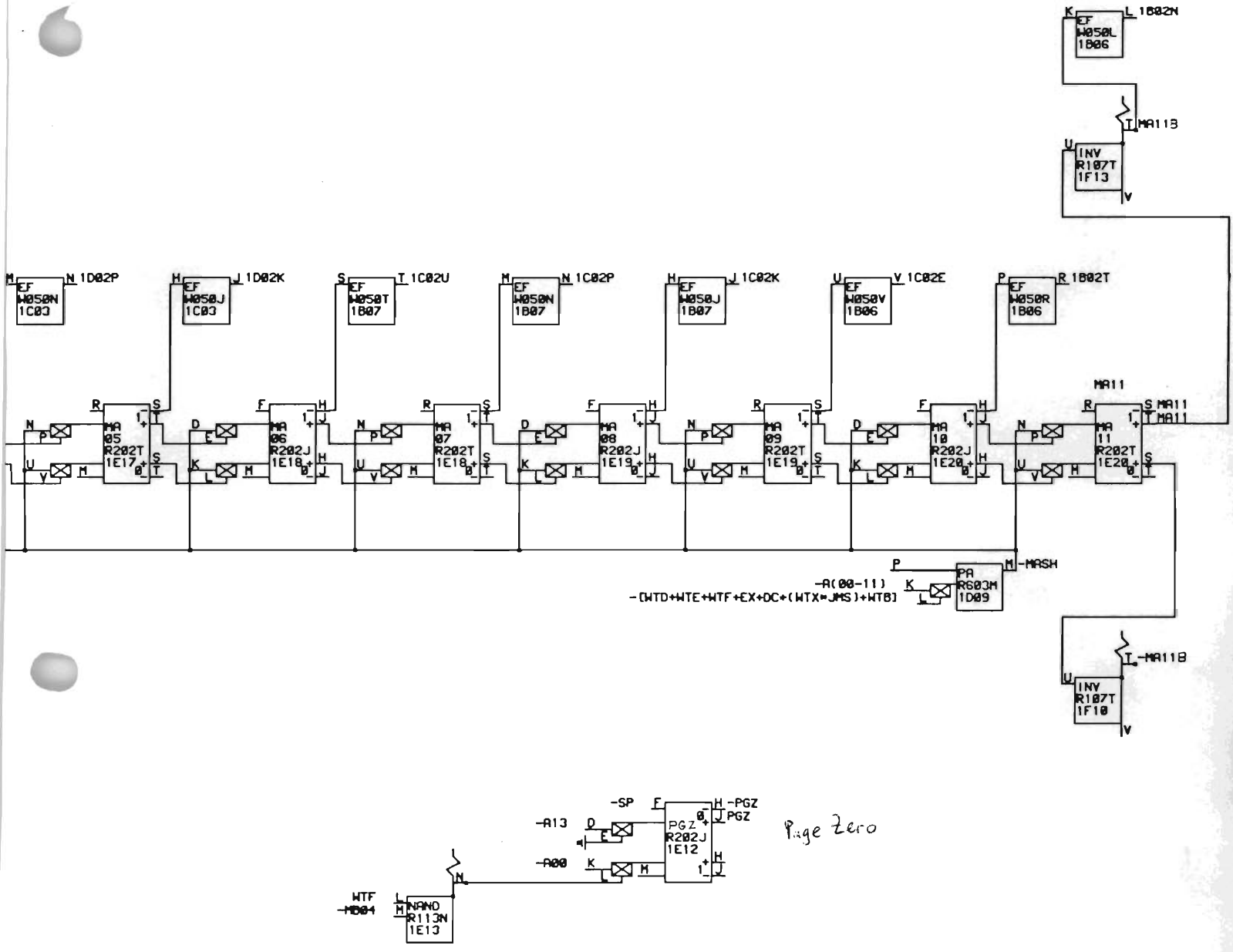
V P INV R107N 1C09

N BT(Ø7-11)

controls transfer of ~~data~~ part to mA. page

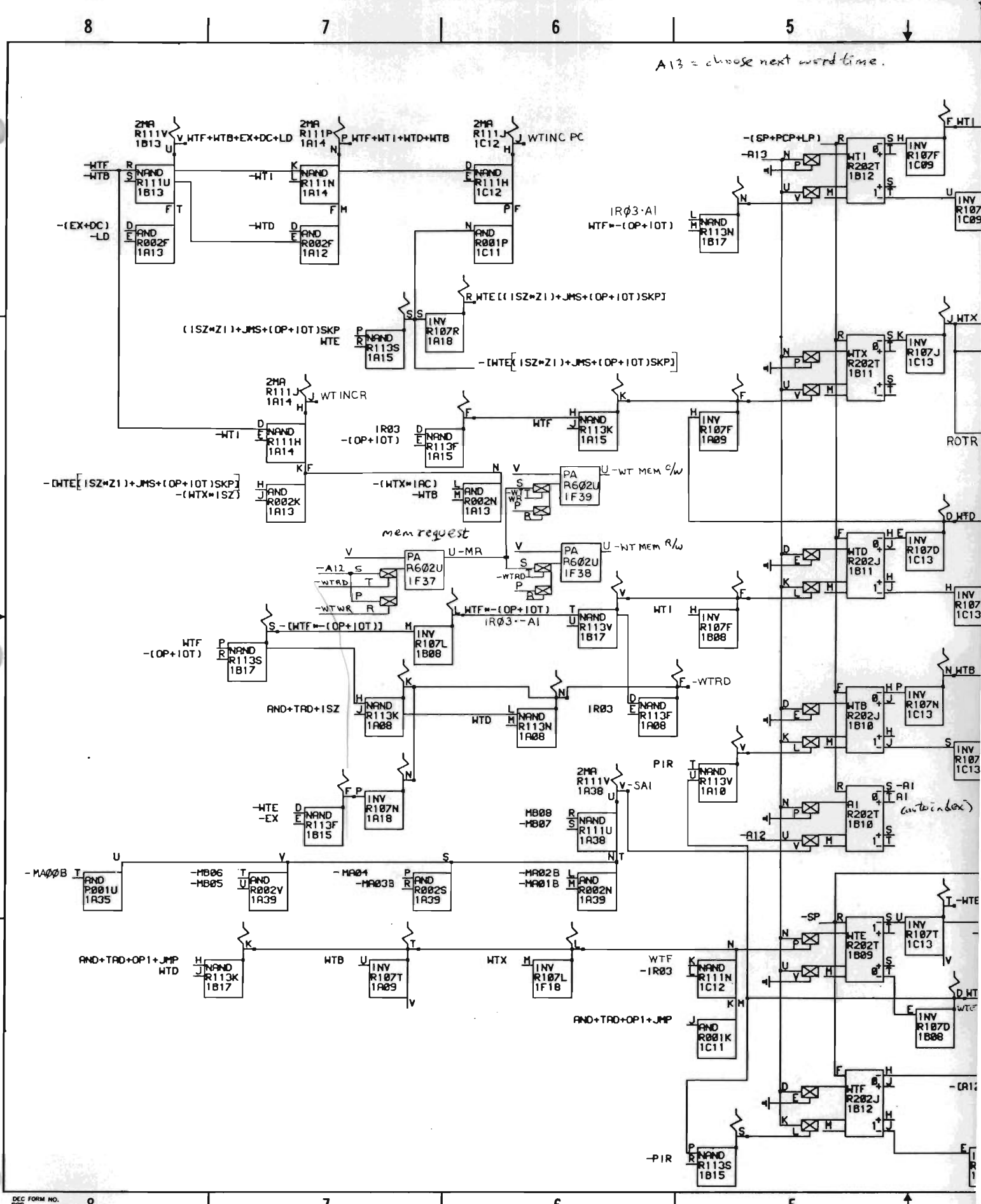


BS-85-04-12
MEM ADDR

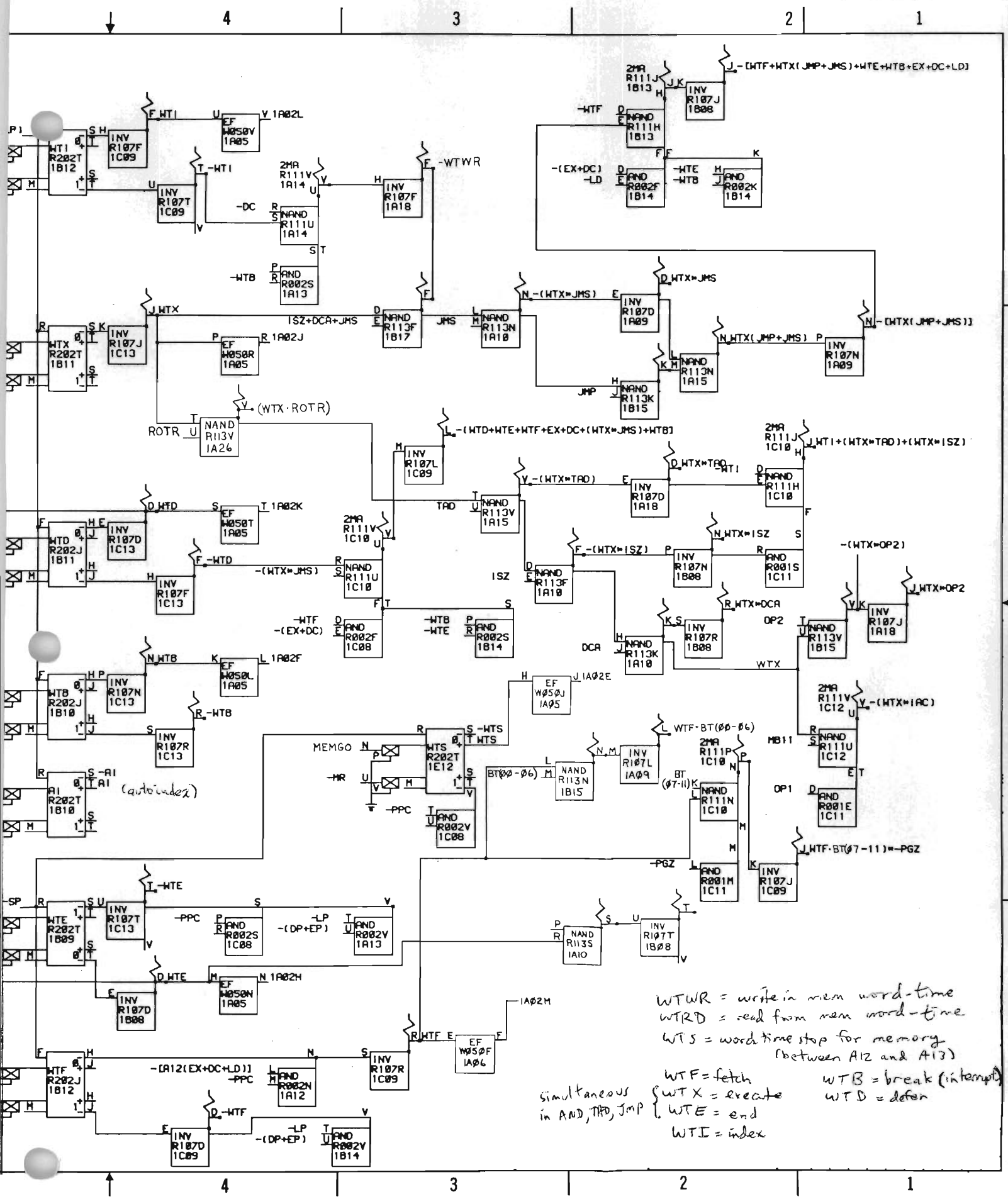

1B02N
MA11B
INV R107T 1F13
1D02P
1D02K
1C02U
1C02P
1C02K
1C02E
1B02T
MA11
MA 05 R202T 1E17
MA 06 R202J 1E18
MA 07 R202T 1E18
MA 08 R202J 1E19
MA 09 R202T 1E19
MA 10 R202J 1E20
MA 11 R202T 1E20
-MASH
-A(00-11)
-(WTD+WTE+WTF+EX+DC+(WTX*JMS)+WTB)
PA R603M 1D09
-MA11B
INV R107T 1F10

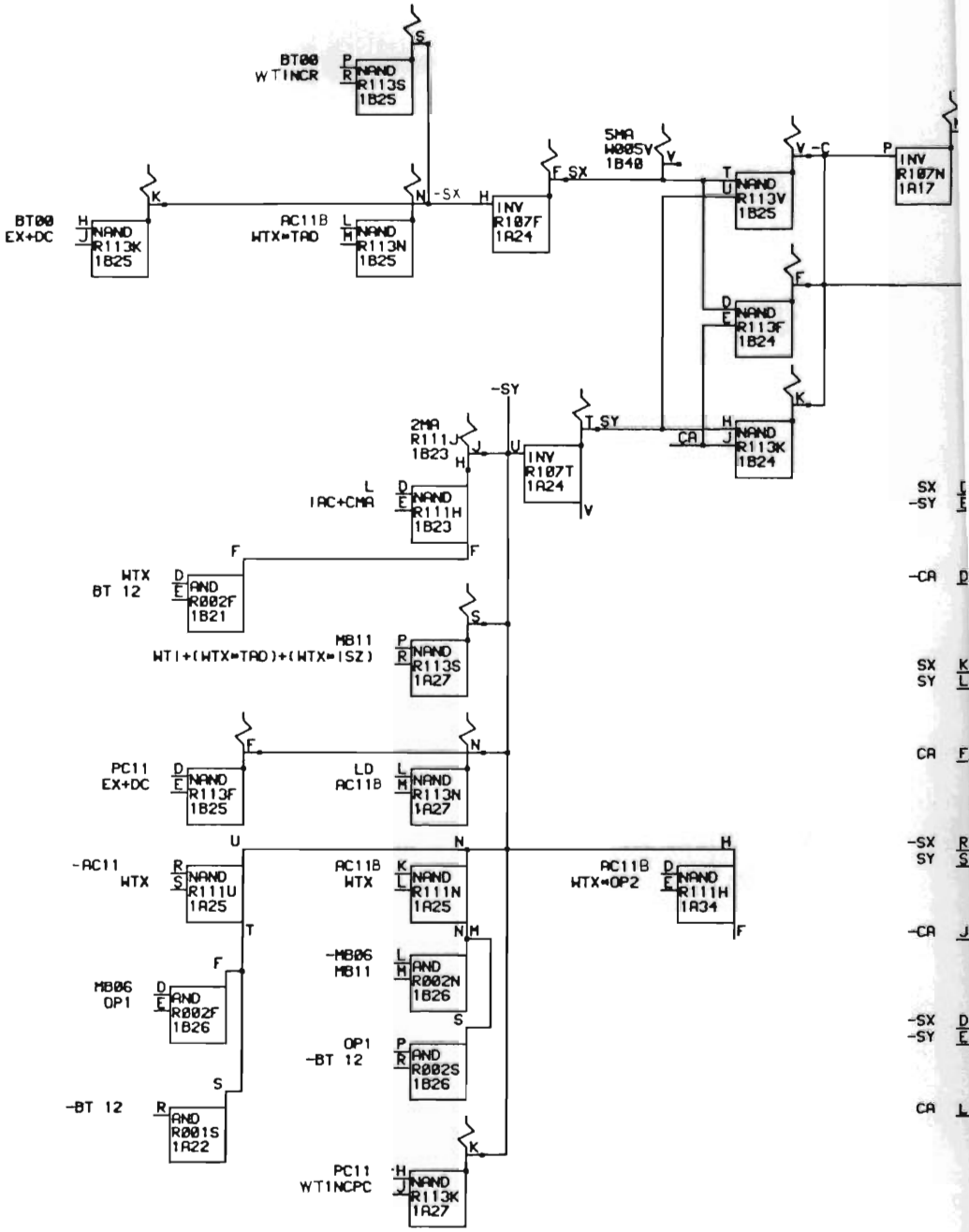
-SP
-A13
-A00
PGZ R202J 1E12
-PGZ
PGZ
WTF
-MB04
NAND R113N 1E13

Page Zero

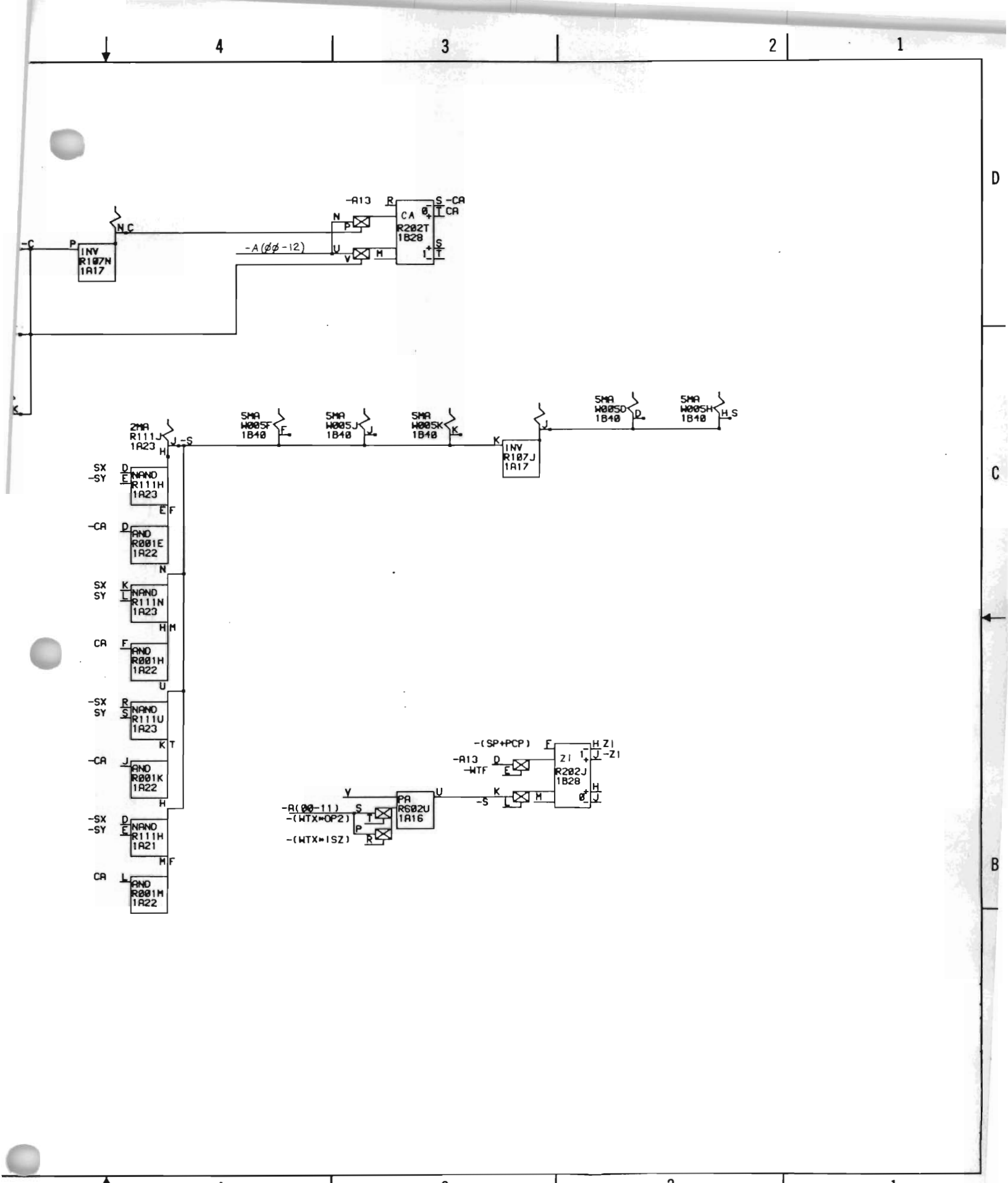


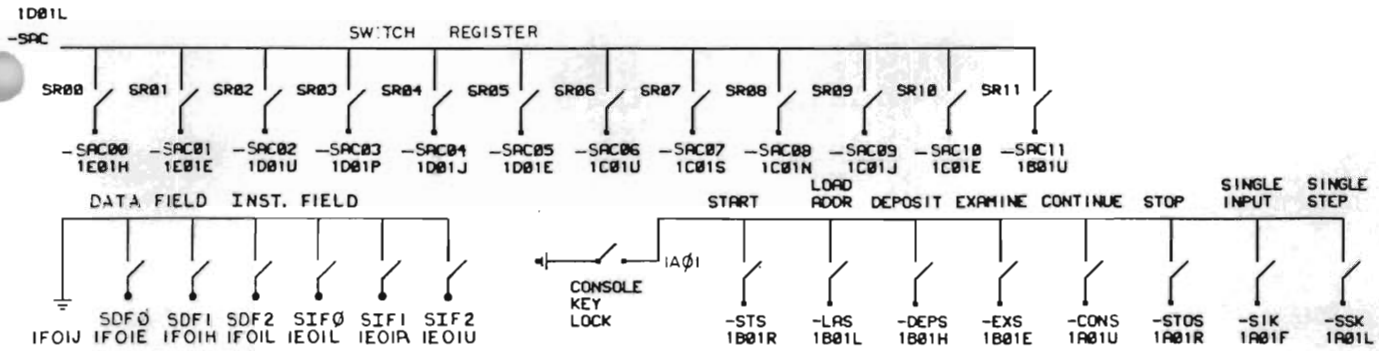
BS-85-0-13
WORD TIMING

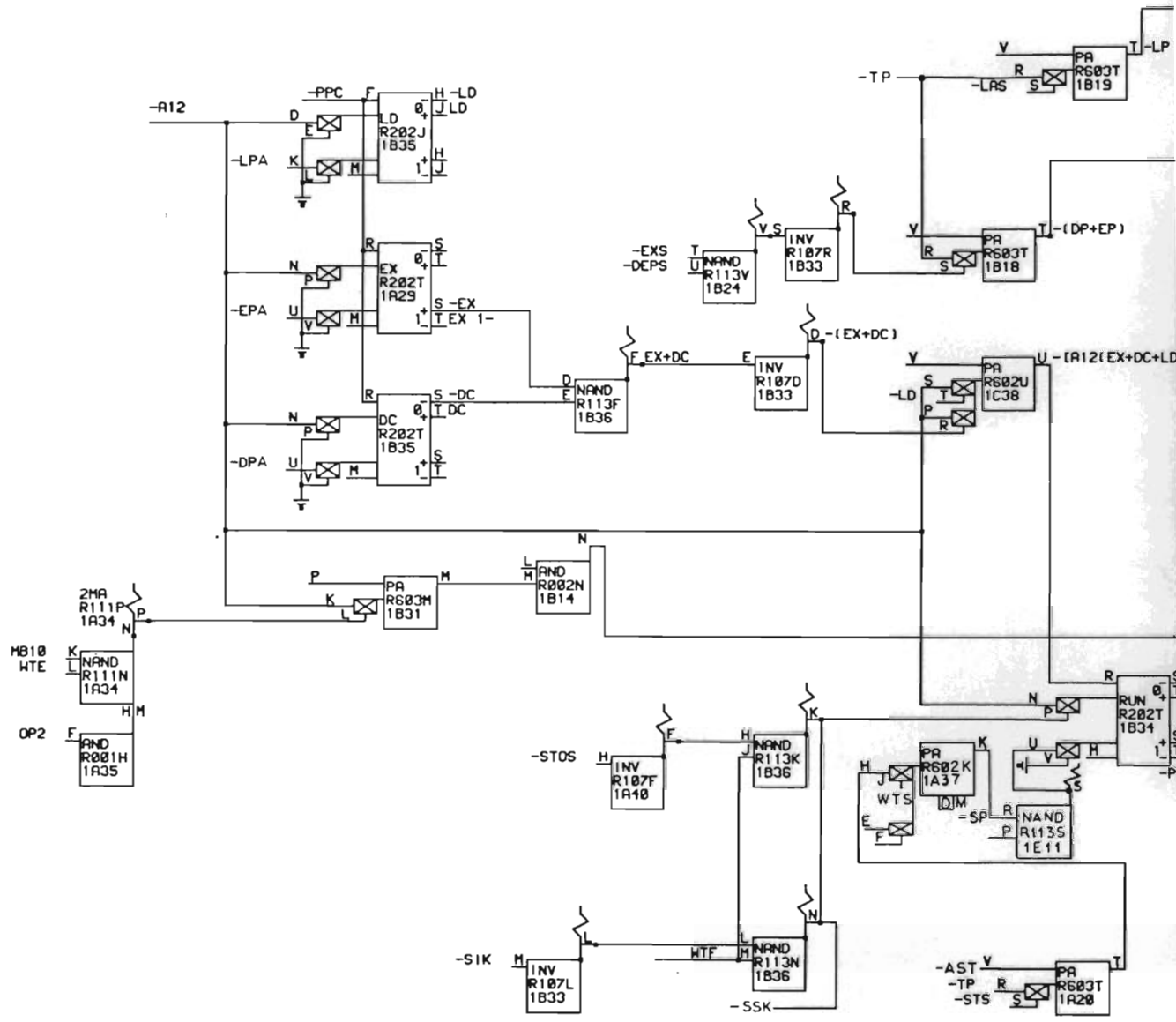

4
3
2
1
D
C
B
A
WTWR = write in mem word-time
WTRD = read from mem word-time
WTS = word time stop for memory (between A12 and A13)
WTF = fetch
WTX = execute
WTE = end
WTI = index
WTB = break (interrupt)
WTD = defer
simultaneous in AND, TAD, JMP
(autoindex)



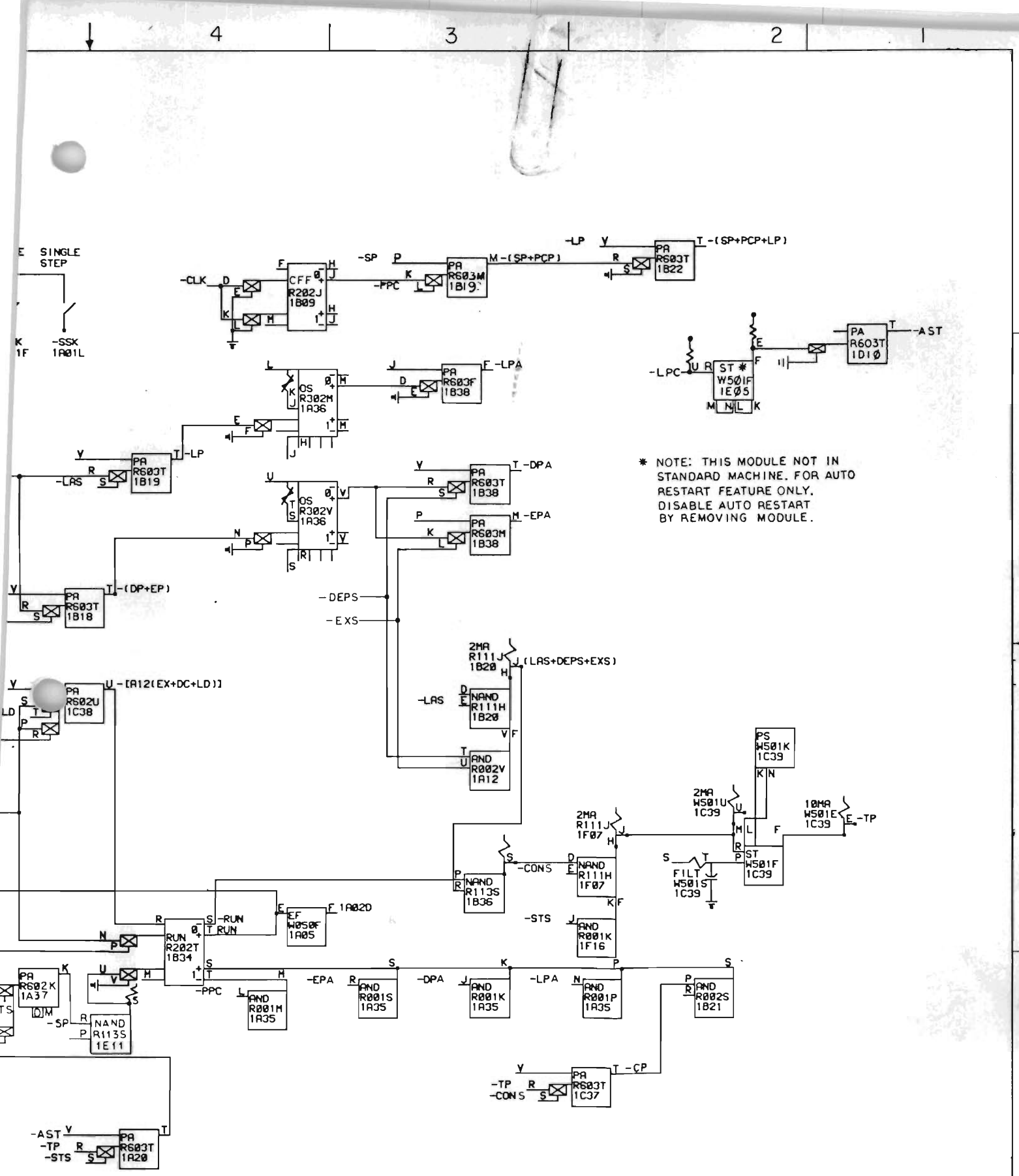
BS-85-0-14
ADDER

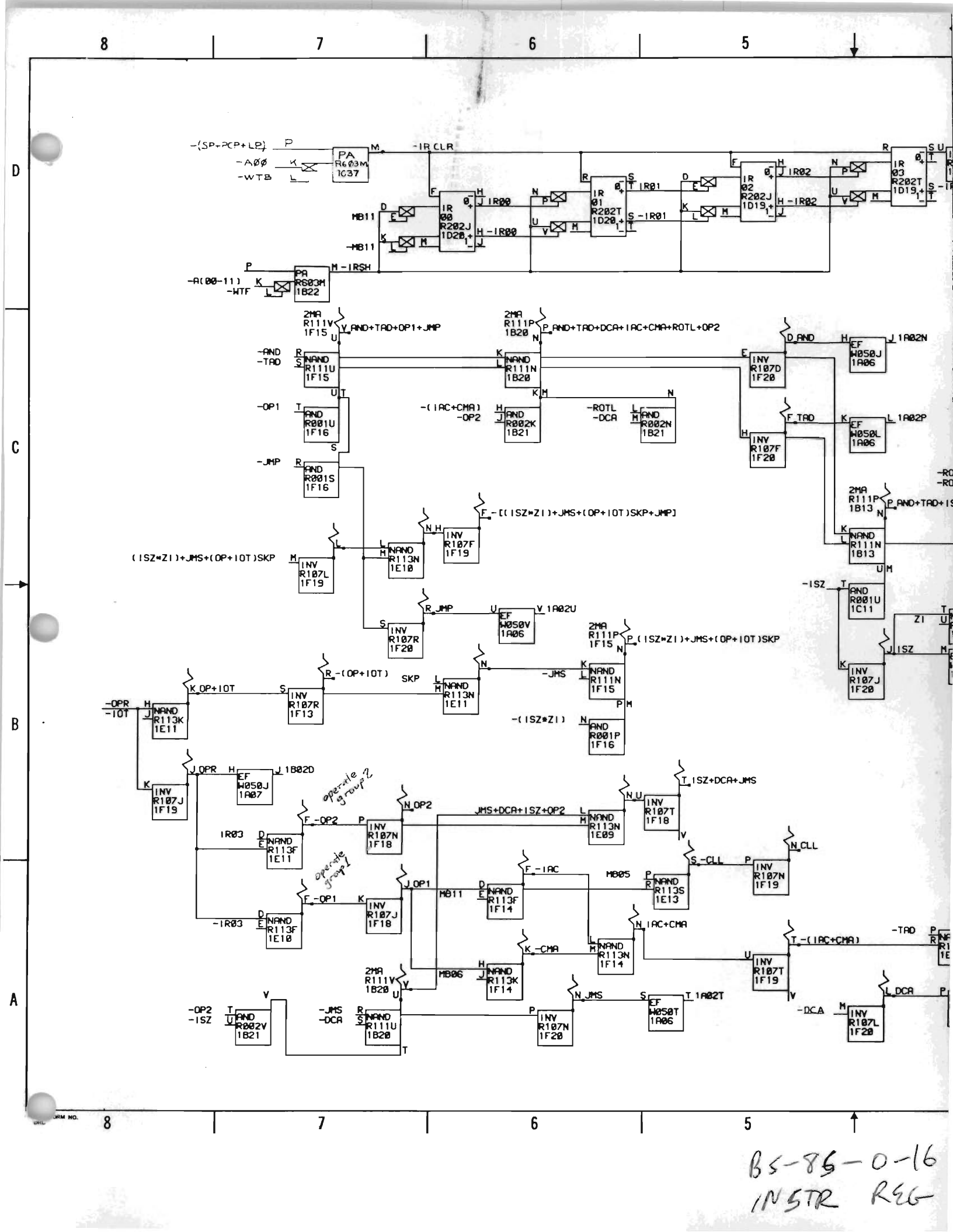

4
3
2
1
D
C
B
-A13
R
S
-CA
CA
R202T
1B28
N
P
-A(ØØ-12)
U
V
M
-C
INV
R107N
1A17
5MA
W005F
1B40
5MA
W005J
1B40
5MA
W005K
1B40
5MA
W005D
1B40
5MA
W005H
1B40
INV
R107J
1A17
2MA
R111J
1A23
-S
SX
-SY
NAND
R111H
1A23
-CA
AND
R001E
1A22
NAND
R111N
1A23
CA
AND
R001H
1A22
-SX
SY
NAND
R111U
1A23
AND
R001K
1A22
-SX
-SY
NAND
R111H
1A21
CA
AND
R001M
1A22
-(SP+PCP)
-A13
-WTF
Z1
R202J
1B28
-Z1
-S
PA
R602U
1A16
-A(ØØ-11)
-(WTX=OP2)
-(WTX=ISZ)



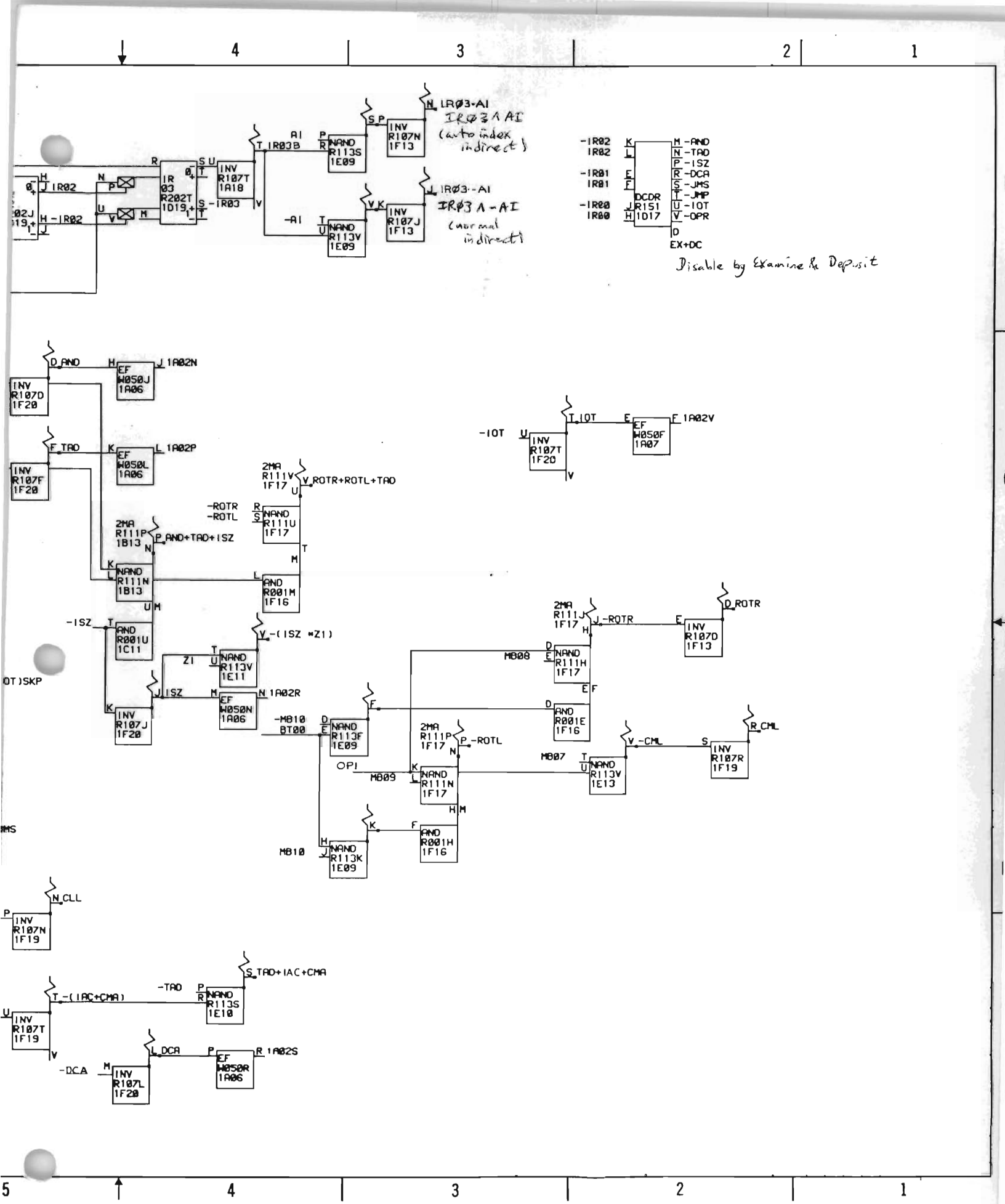


BS-85-0-15
CONTROL

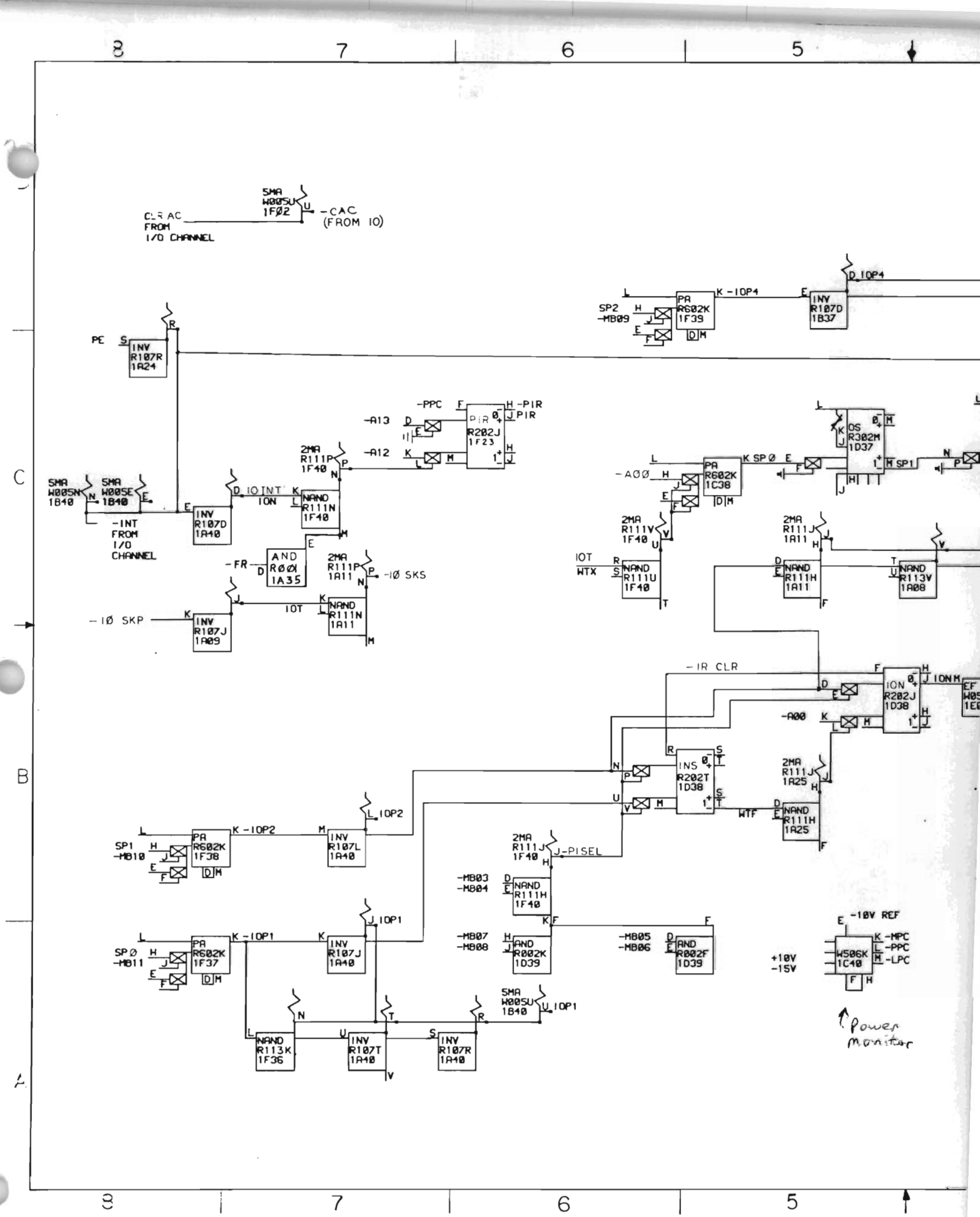

SINGLE STEP
-SSK 1A01L
-CLK
CFF R202J 1B09
-SP
-PPC
PA R603M 1B19
M-(SP+PCP)
-LP
PA R603T 1B22
T-(SP+PCP+LP)
PA R603T 1D10
-AST
-LPC
ST * W501F 1E05
OS R302M 1A36
PA R603F 1B38
-LPA
PA R603T 1B19
-LAS
-LP
OS R302V 1A36
PA R603T 1B38
-DPA
PA R603M 1B38
-EPA
PA R603T 1B18
-(DP+EP)
-DEPS
-EXS
2MA R111J 1B20
(LAS+DEPS+EXS)
NAND R111H 1B20
AND R002V 1A12
PA R602U 1C38
-[A12(EX+DC+LD)]
PS W501K 1C39
2MA W501U 1C39
10MA W501E 1C39
-TP
2MA R111J 1F07
NAND R111H 1F07
-CONS
FILT W501S 1C39
ST W501F 1C39
NAND R113S 1B36
-STS
AND R001K 1F16
EF W050F 1A05
1A02D
RUN R202T 1B34
-RUN
RUN
-PPC
-EPA
-DPA
-LPA
AND R001M 1A35
AND R001S 1A35
AND R001K 1A35
AND R001P 1A35
AND R002S 1B21
PA R602K 1A37
-SP
NAND R113S 1E11
PA R603T 1C37
-CP
-TP
-CONS
-AST
-TP
-STS
PA R603T 1A20
* NOTE: THIS MODULE NOT IN STANDARD MACHINE. FOR AUTO RESTART FEATURE ONLY. DISABLE AUTO RESTART BY REMOVING MODULE.



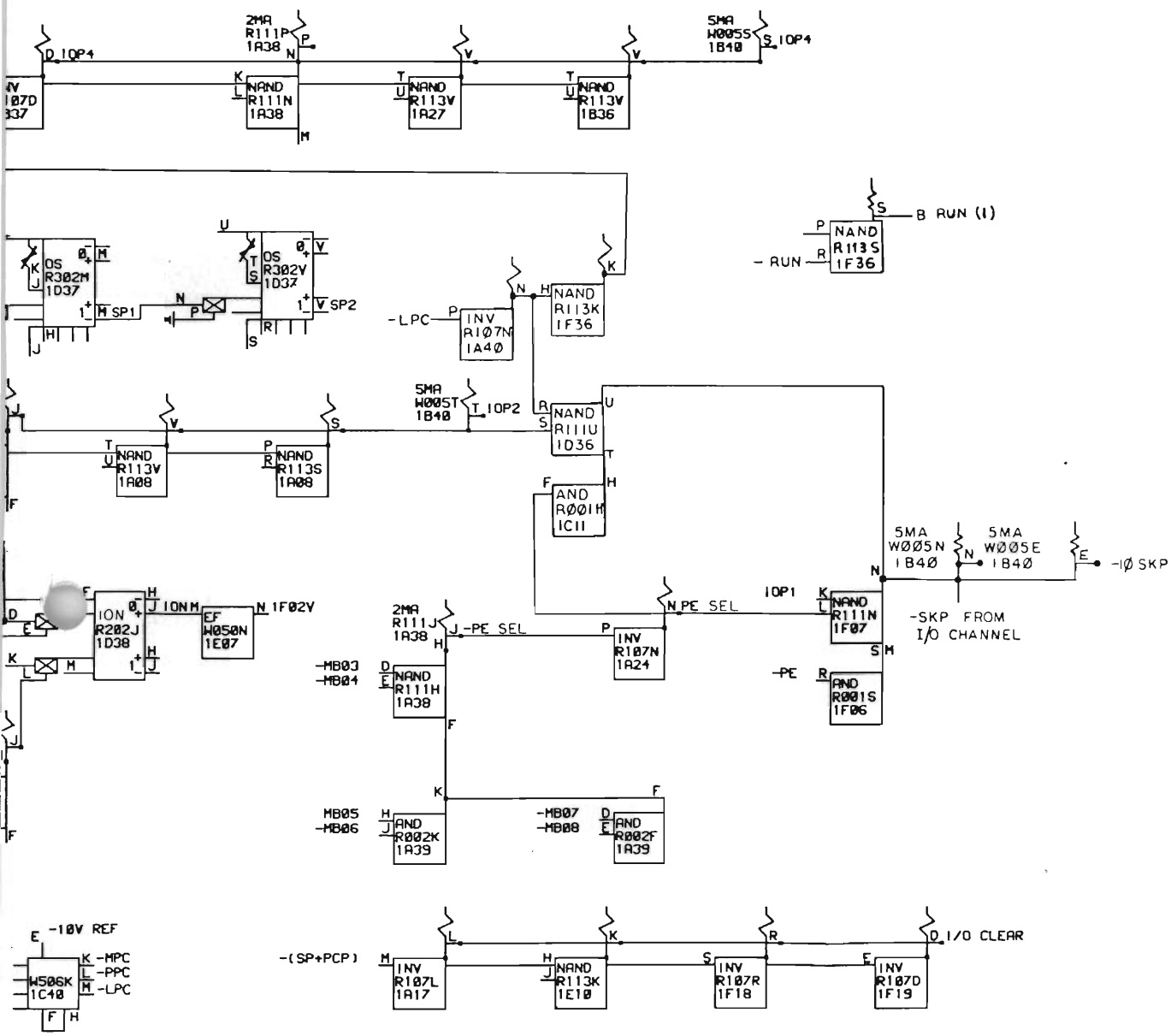
BS-86-0-16
INSTR REG



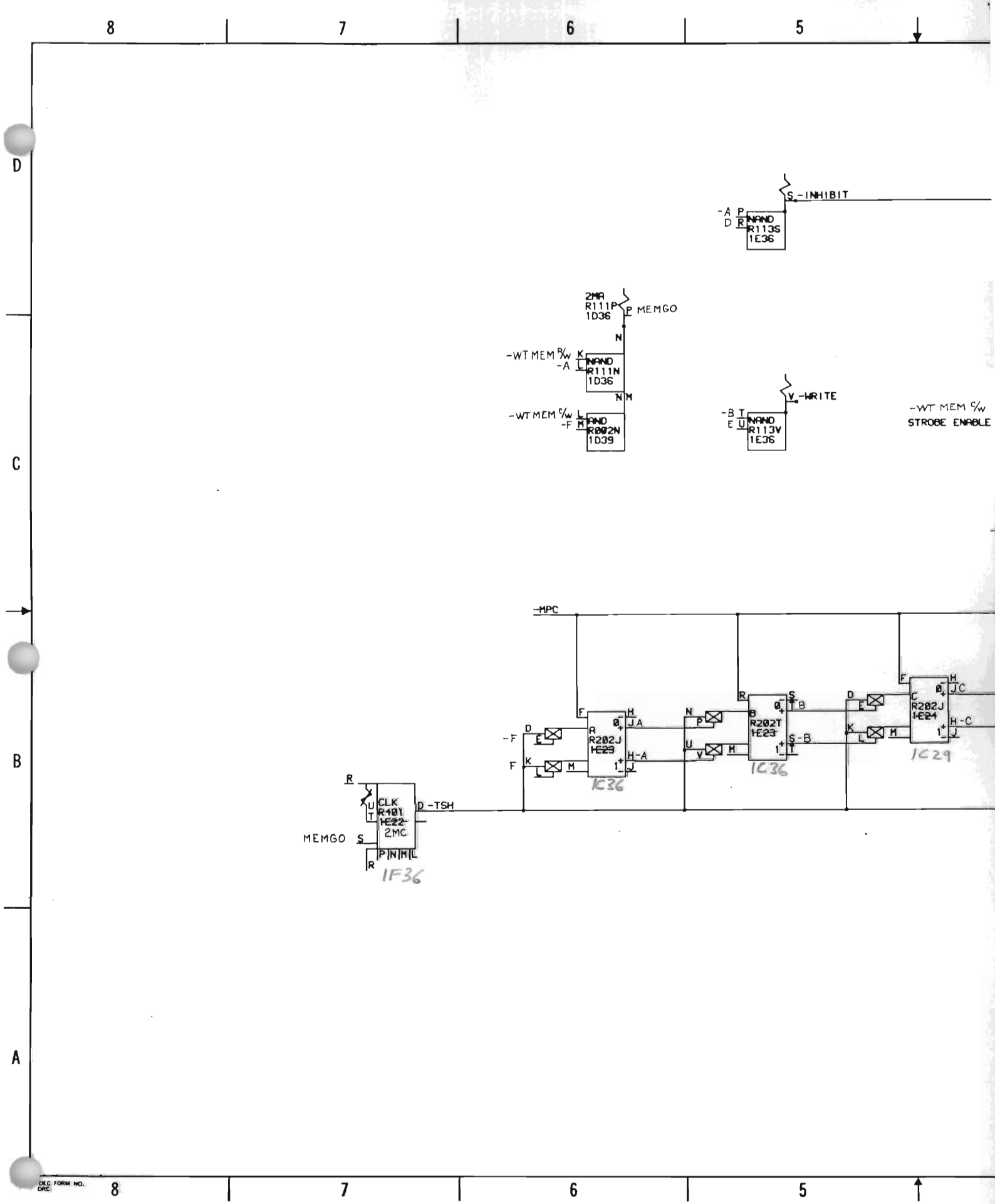
Instruction Register D-BS-8S-0-16



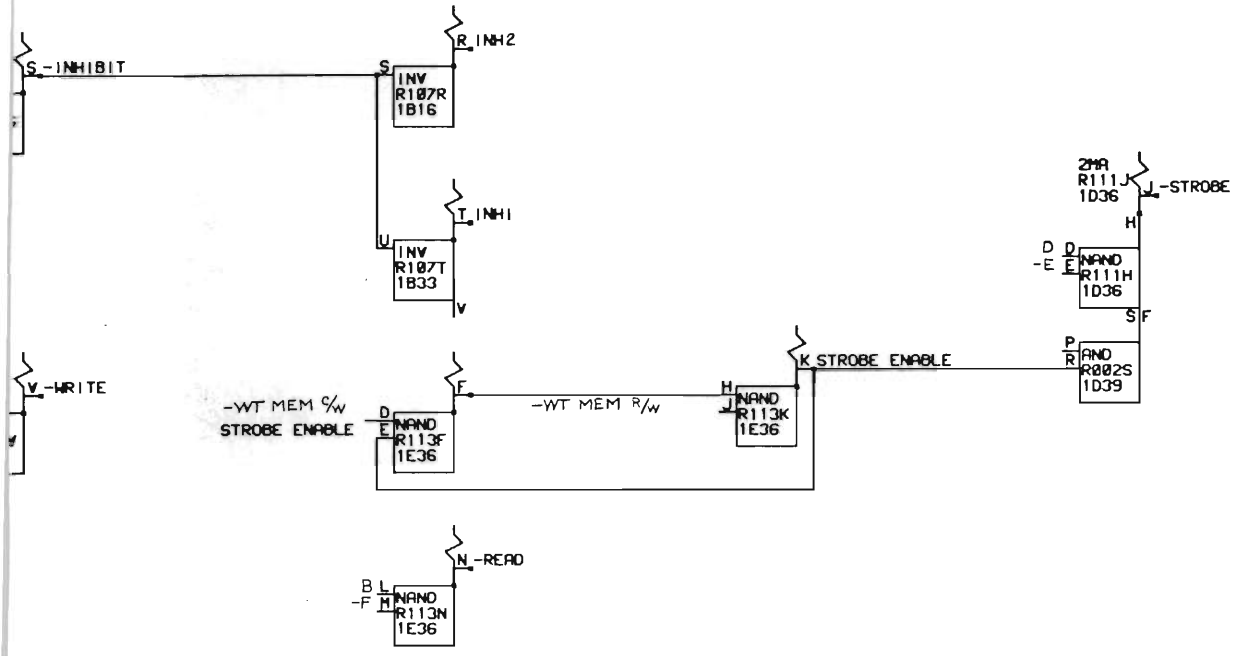
85-85-0-17
IN OUT

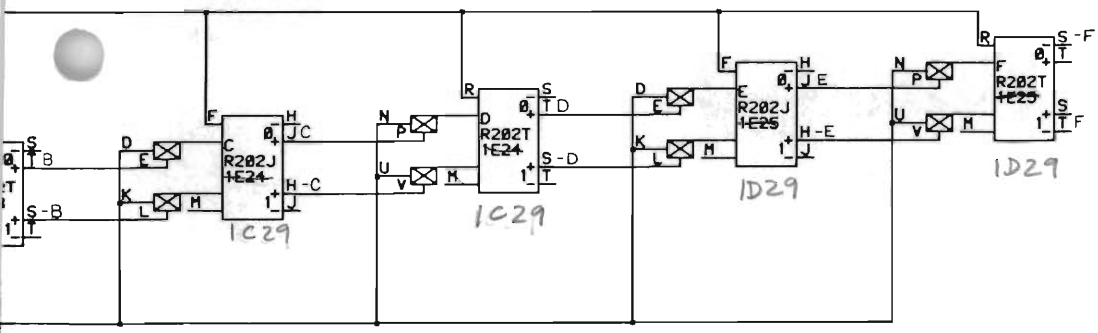


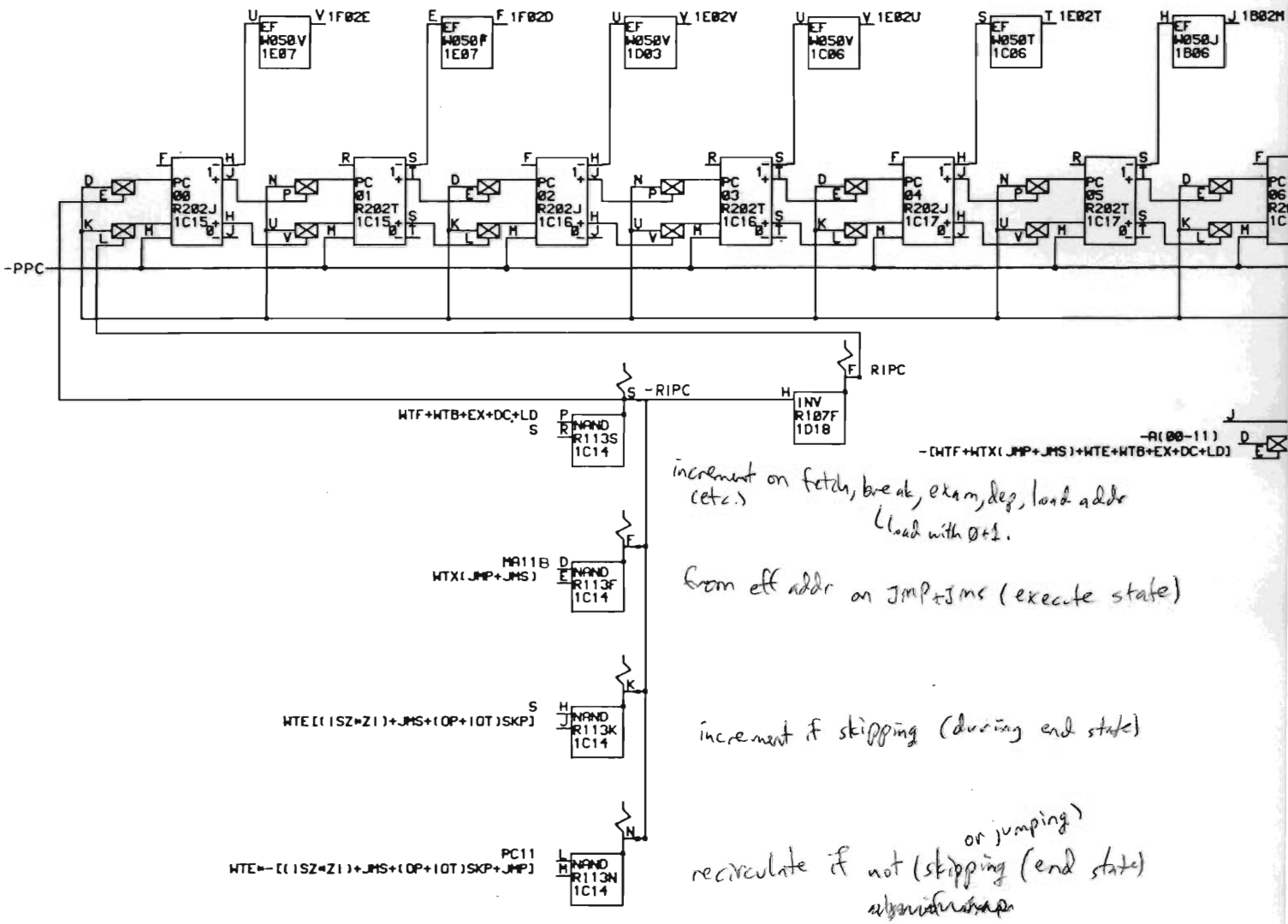
In-out D-BS-8S-0-17



BS-85-0-18
MEM CTL (4K)


S -INHIBIT
INV R107R 1B16
R INH2
INV R107T 1B33
T INH1
V -WRITE
-WT MEM S/W STROBE ENABLE
NAND R113F 1E36
-WT MEM R/W
NAND R113K 1E36
K STROBE ENABLE
2MA R111J 1D36
J -STROBE
NAND R111H 1D36
AND R002S 1D39
N -READ
NAND R113N 1E36


R202J 1E24
1C29
R202T 1E24
1C29
R202J 1E25
1D29
R202T 1E25
1D29
S-B
H-C
S-D
H-E
S-F



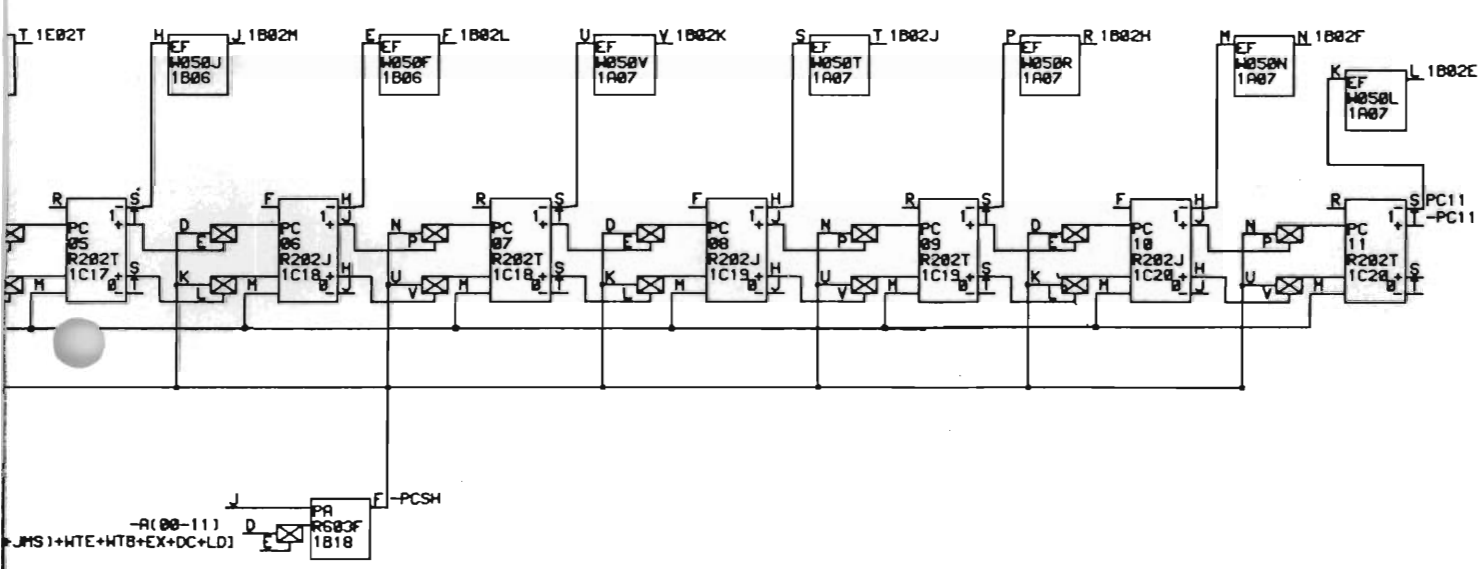
increment on fetch, break, exam, dep, load addr (etc.)
(Load with Ø+1.

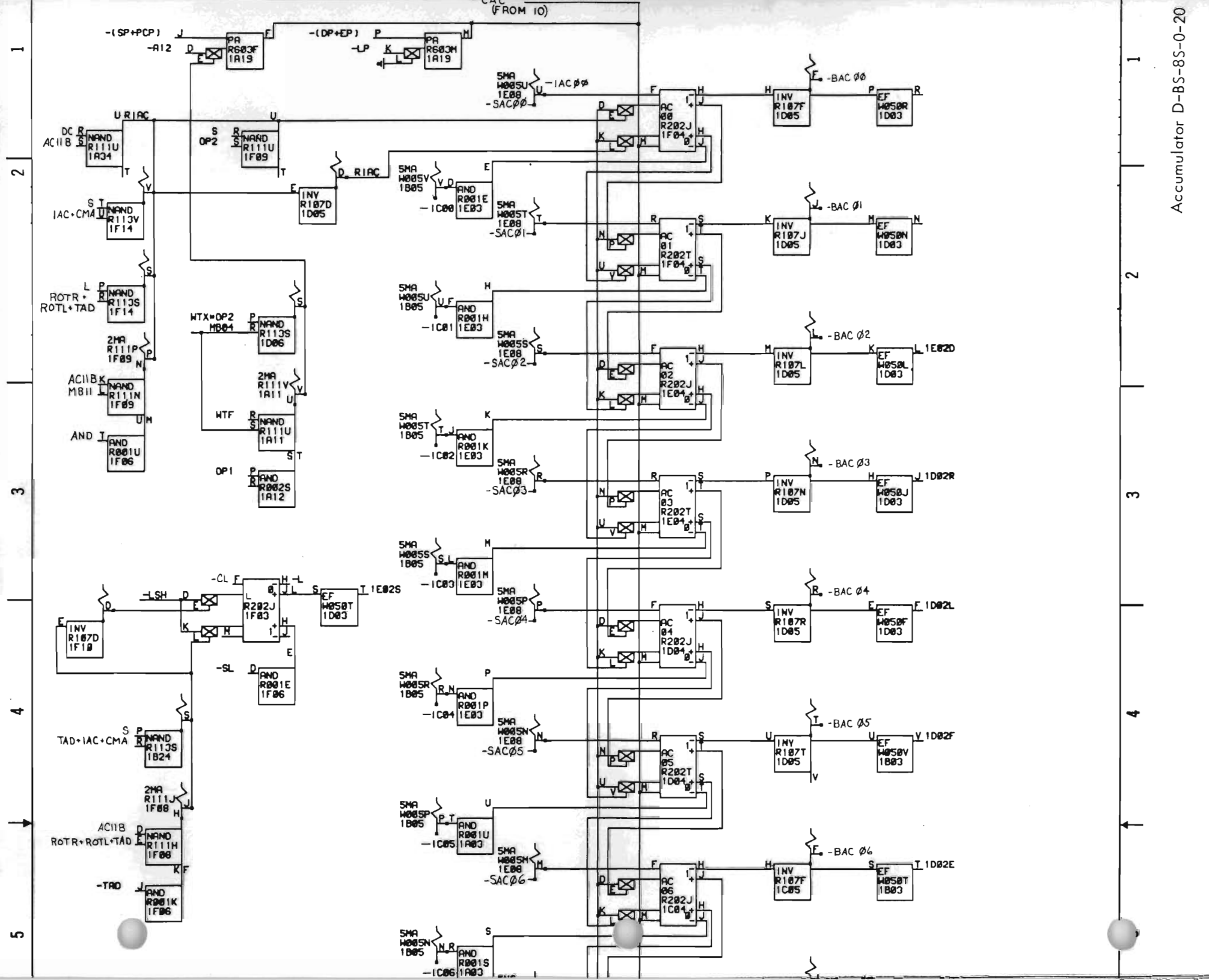
from eff addr on JMP+JMS (execute state)

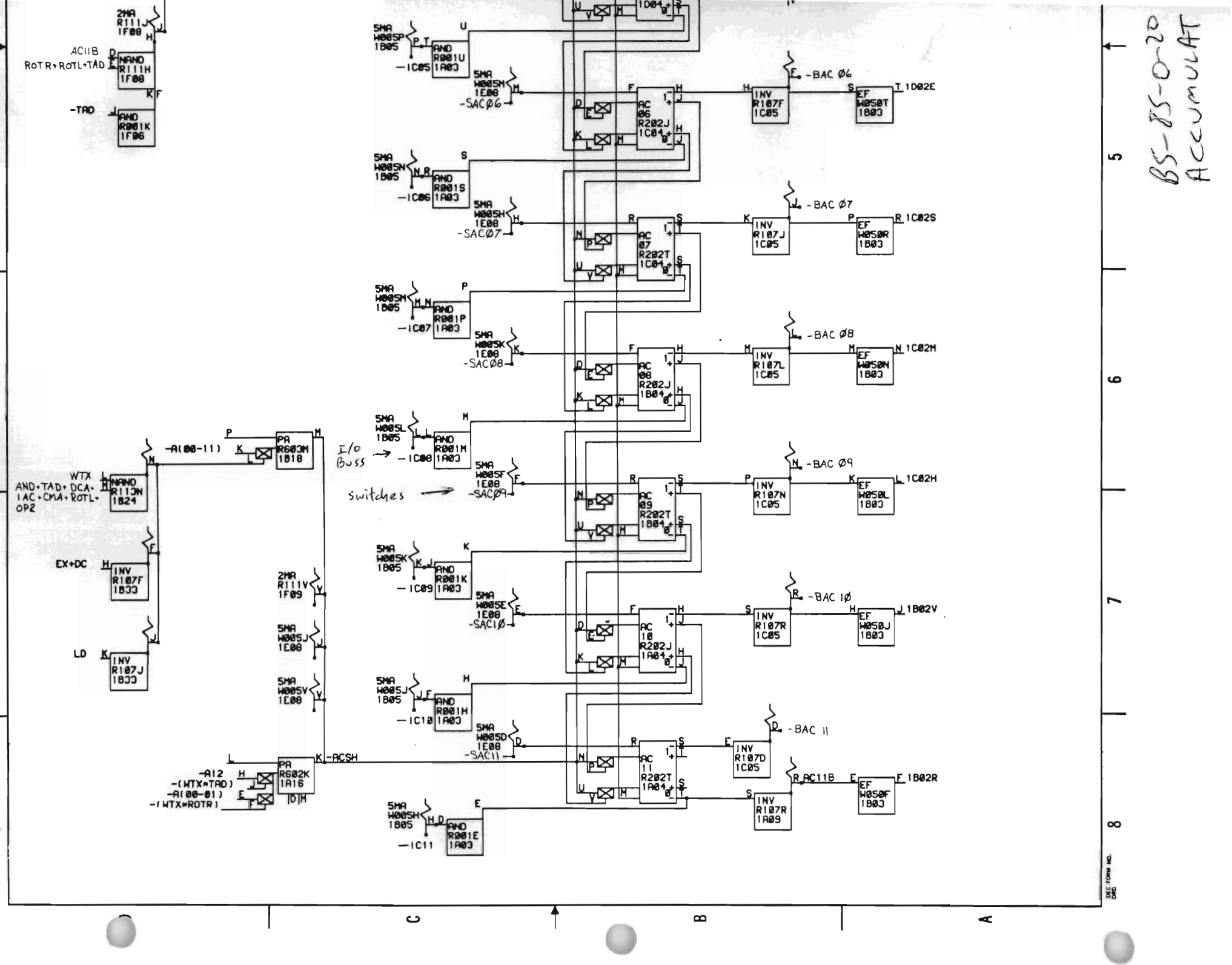
increment if skipping (during end state)

recirculate if not (skipping (end state) or jumping)

85-85-0-19
PROG CTR

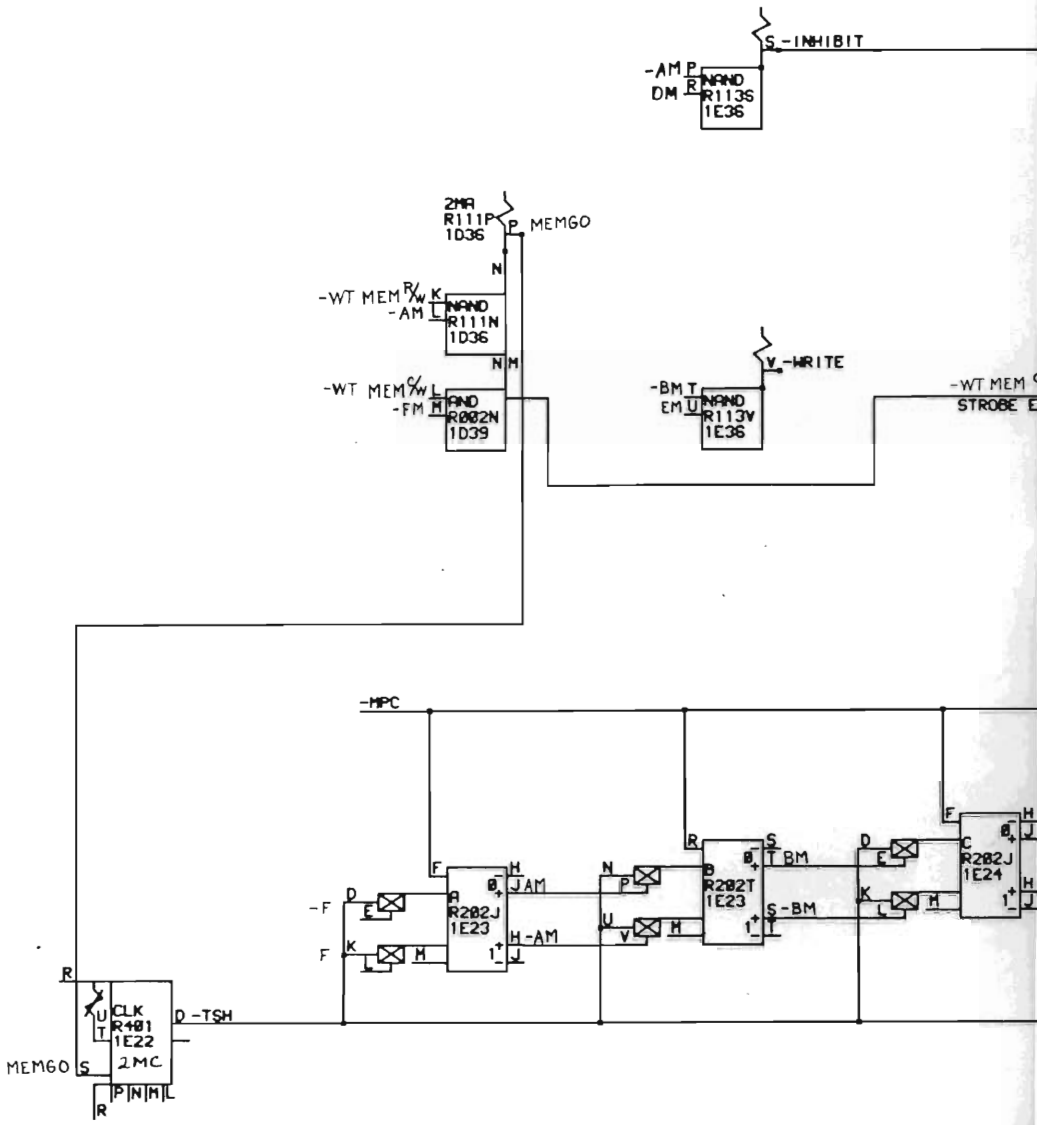

T 1E02T
H EF W050J 1B06 J 1B02M
E EF W050F 1B06 F 1B02L
U EF W050V 1A07 V 1B02K
S EF W050T 1A07 T 1B02J
P EF W050R 1A07 R 1B02H
M EF W050N 1A07 N 1B02F
K EF W050L 1A07 L 1B02E
PC 05 R202T 1C17
PC 06 R202J 1C18
PC 07 R202T 1C18
PC 08 R202J 1C19
PC 09 R202T 1C19
PC 10 R202J 1C20
PC 11 R202T 1C20
PC11
-PC11
-A(00-11)
PA RG03F 1B18
-PCSH
JMS)+WTE+WTB+EX+DC+LDI


(FROM 10)
-(SP+PCP)
-A12
-(DP+EP)
-LP
-IAC ØØ
-SAC ØØ
-BAC ØØ
-BAC Ø1
-BAC Ø2
-BAC Ø3
-BAC Ø4
-BAC Ø5
-BAC Ø6
DC ACIIB
OP2
IAC
IAC+CMA
ROTR+ROTL+TAD
WTX=OP2
MB04
ACIIB MBII
WTF
AND
OP1
-CL
-LSH
-SL
TAD+IAC+CMA
ACIIB ROTR+ROTL+TAD
-TAD
-IC00
-IC01
-IC02
-IC03
-IC04
-IC05
-IC06
-SAC Ø1
-SAC Ø2
-SAC Ø3
-SAC Ø4
-SAC Ø5
-SAC Ø6


BS-85-D-20
ACCUMULAT
AC11B
ROTR+ROTL+TAD
NAND R111H 1F08
-TAD
AND R001K 1F06
2MA R111 1F08
WTX
AND+TAD+DCA+IAC+CMA+ROTL+OP2
NAND R113N 1B24
EX+DC
INV R107F 1B33
LD
INV R107J 1B33
2MA R111V 1F09
5MA W005J 1E08
5MA W005V 1E08
-A(00-11)
PA R603M 1B18
I/O Buss
switches
-A12
-(WTX*TAD)
-A(00-01)
-(WTX*ROTR)
PA R602K 1A16
-ACSH
5MA W005P 1B05
AND R001U 1A03
-IC05
5MA W005H 1E08
-SAC06
AC 06 R202J 1C04
INV R107F 1C05
EF W050T 1B03
-BAC 06
1D02E
5MA W005N 1B05
AND R001S 1A03
-IC06
5MA W005H 1E08
-SAC07
AC 07 R202T 1C04
INV R107J 1C05
EF W050R 1B03
-BAC 07
1C02S
5MA W005M 1B05
AND R001P 1A03
-IC07
5MA W005K 1E08
-SAC08
AC 08 R202J 1B04
INV R107L 1C05
EF W050N 1B03
-BAC 08
1C02M
5MA W005L 1B05
AND R001M 1A03
-IC08
5MA W005F 1E08
-SAC09
AC 09 R202T 1B04
INV R107N 1C05
EF W050L 1B03
-BAC 09
1C02H
5MA W005K 1B05
AND R001K 1A03
-IC09
5MA W005E 1E08
-SAC10
AC 10 R202J 1A04
INV R107R 1C05
EF W050J 1B03
-BAC 10
1B02V
5MA W005J 1B05
AND R001M 1A03
-IC10
5MA W005D 1E08
-SAC11
AC 11 R202T 1A04
INV R107D 1C05
INV R107R 1A09
EF W050F 1B03
-BAC 11
AC11B
1B02R
5MA W005H 1B05
AND R001E 1A03
-IC11

INOPERATIVE

See #18

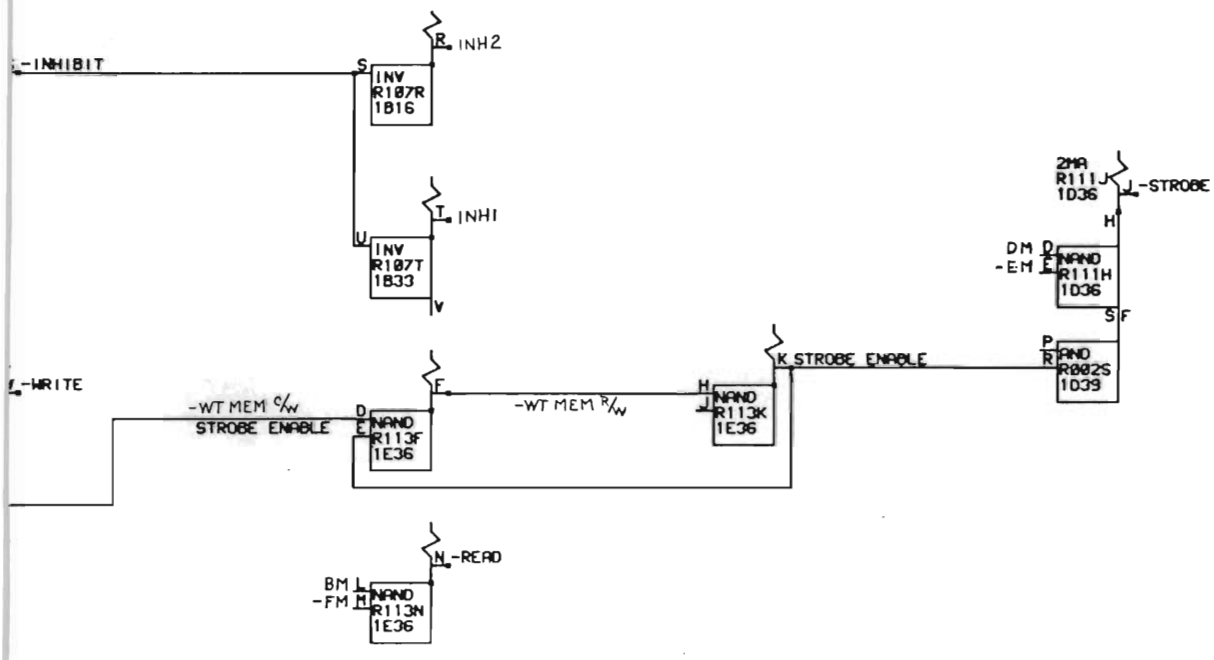


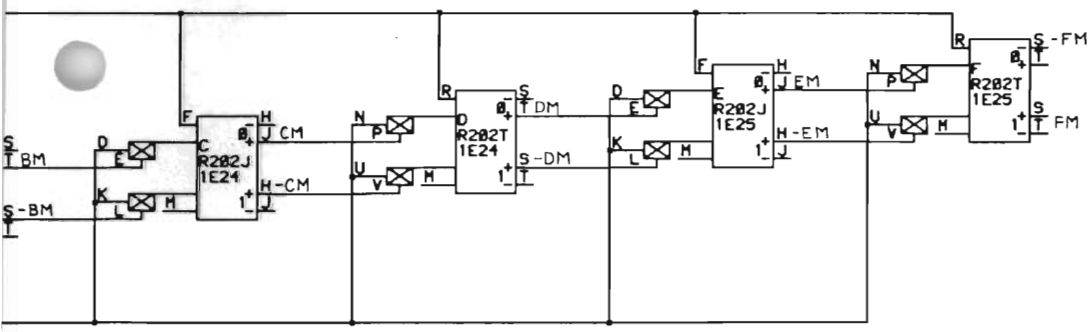
85-85-0-22

MEM CTL (8K)

INOPERATIVE

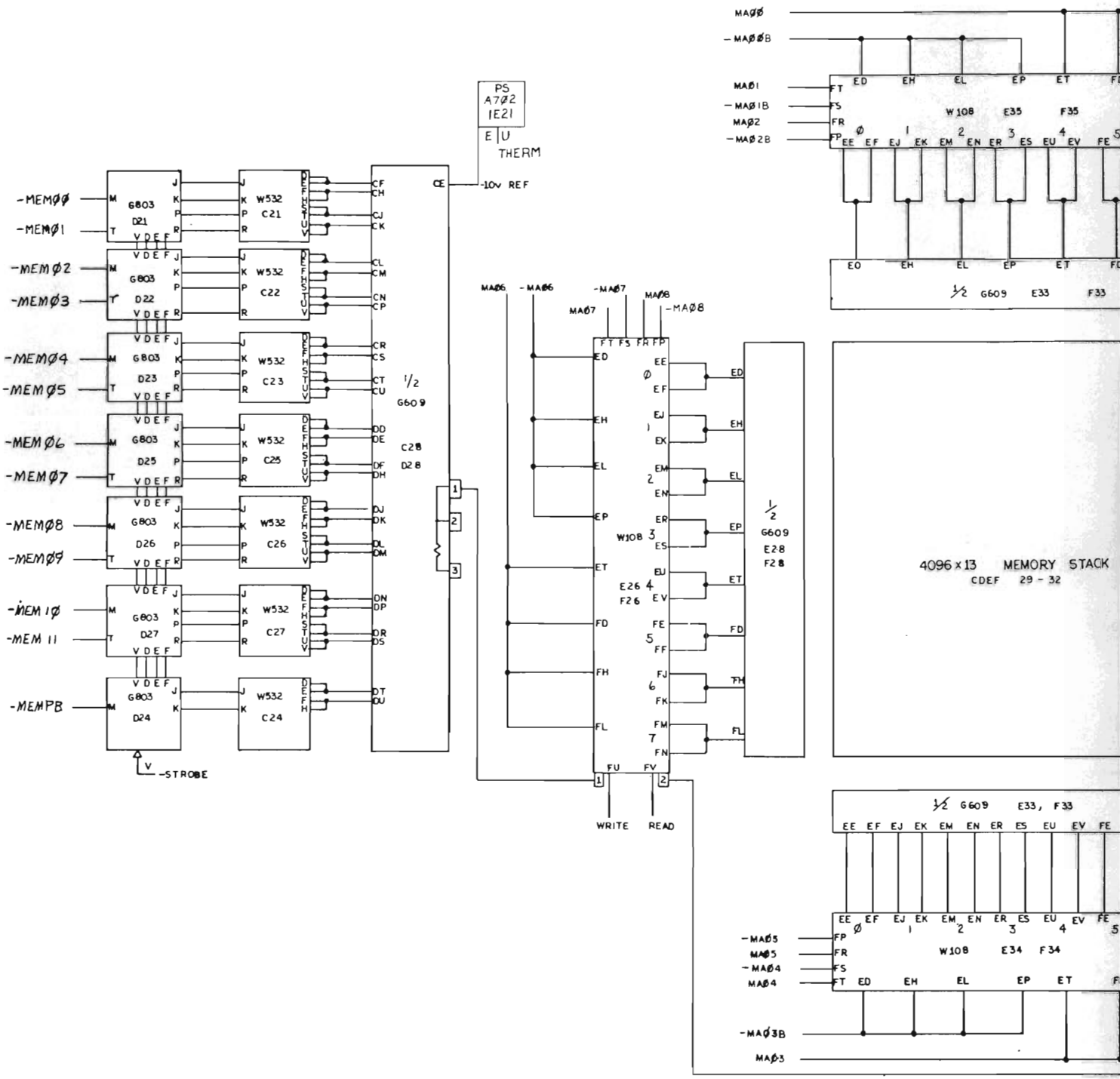
See #18





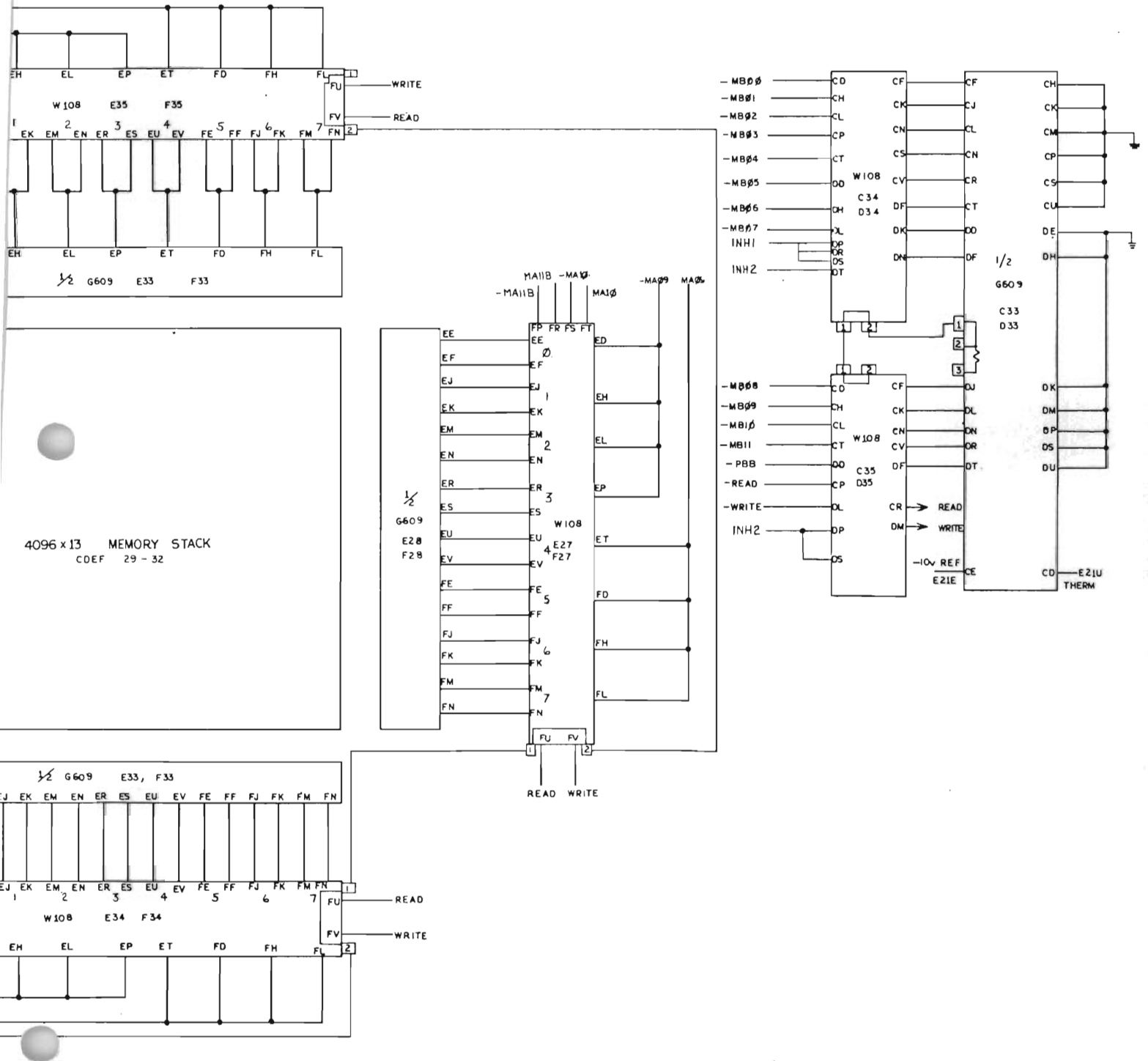
INOPERATIVE

See #4



85-85-0-23
MEM BLOCK
DIAG (8K)

INOPERATIVE
See #4



Memory Block Diagram (8K) D-BS-8S-0
-23

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
			R00I	R2Ø2	WØ5Ø	WØ5Ø	WØ5Ø	RII3	RIØ7	RII3	RIII	R00Ø2	R00Ø2	RIII	RII3	R6Ø2	RIØ7	RIØ7	R6Ø3	R6Ø3	RIII	R00I
A			ACII	AC1Ø	IAØ2D	IAØ2M	IAØ2V	RDS	WTX *JMS	-(WTX *ISZ)	IOP2	IAI4M	IBI3T	INCR	WTX	ACSH	BMB Ø6 (I)	WTX *TAD	RAC	SAC	S	
			ACIØ		IAØ2E	IAØ2N	IAØ2O		WTX	WTX *DCA	IOP2		INCR		WTX		BMB Ø6(Ø)	WRS				
			ACØ9		IAØ2F	IAØ2P	IBØ2E		SKS	-(WTX *JMS)	SKS	WTF		IAI4P	WTX (JMP +JMS)		S	WTX +OP2	RAC	SAC	S	S
			ACØ8	AC11	IAØ2H	IAØ2R	IBØ2F		WTF BT Ø6		SKS						I/O CLR	RIMA			RL	
			ACØ7		IAØ2J	IAØ2S	IBØ2H	IOP2	-WTX +JMP	IBØ8U	RAC	RAC	WRS	WRS	INCPC	ZI	C	RDS	RAC	SAC	LSH	LSH
			ACØ6		IAØ2K	IAØ2T	IBØ2J		AC11								BMB Ø7(1)	IAI8R		SP		SY
			ACØ5		IAØ2L	IAØ2U	IBØ2K	IOP2	WTE	WTB	RAC	LAS + DEPS +EXS	WTE		-(WTX +TAD)		BMB Ø8(1)	IRØ3				RL
			WØ5Ø	R2Ø2	WØØ5	WØ5Ø	WØ5Ø	RIØ7	R2Ø2	R2Ø2	R2Ø2	R2Ø2	R111	R00Ø2	RII3	RIØ7	RII3	R6Ø3	R6Ø3	RIII	R00Ø2	R6Ø
B			IBØ2R	ACØ8	MAØ3 MBØ6	IBØ2L	ICØ2F	WTE	SP	WTB	WTD	WTF		IBØ8J	RDS	WTS	WRS	PCSH		LAS + DEPS + EXS	SY	
			IBØ2V		-IC11	IBØ2M	ICØ2K	WTD					IBØ8K		WTX+ (JMP+ JMS)	MBII	WTE				IB2ØM	
			ICØ2H		-IC1Ø											-(PE SET)				IB2ØP		
			ICØ2M		-IC09 -IC08	IBØ2N	ICØ2L	IBØ8J					IBI3P	RUN	WTF BT ØØ-Ø6	MBSH	WTI	ACSH	SP		IB2ØP	IRSH
			ICØ2S		-IC07 -IC06	IBØ2P	ICØ2P	IBØ8L								RIMB						
			IDØ2E	ACØ9	-IC05 -IC04	IBØ2T	ICØ2R	WTX *ISZ	WTE	AI	WTX	WTI	IBI3V	ICIØT	WTF	INHIB 2	IBI7S	-(DP + EP)	LP	IB2ØV	RUN	-(SP
			IDØ2F		-IC03 -IC02 -IC01 -IC00	IBØ2U	ICØ2S	WTX *DCA							WTX +OP2	MBSH	WTD				IB2ØV	PCP LP)

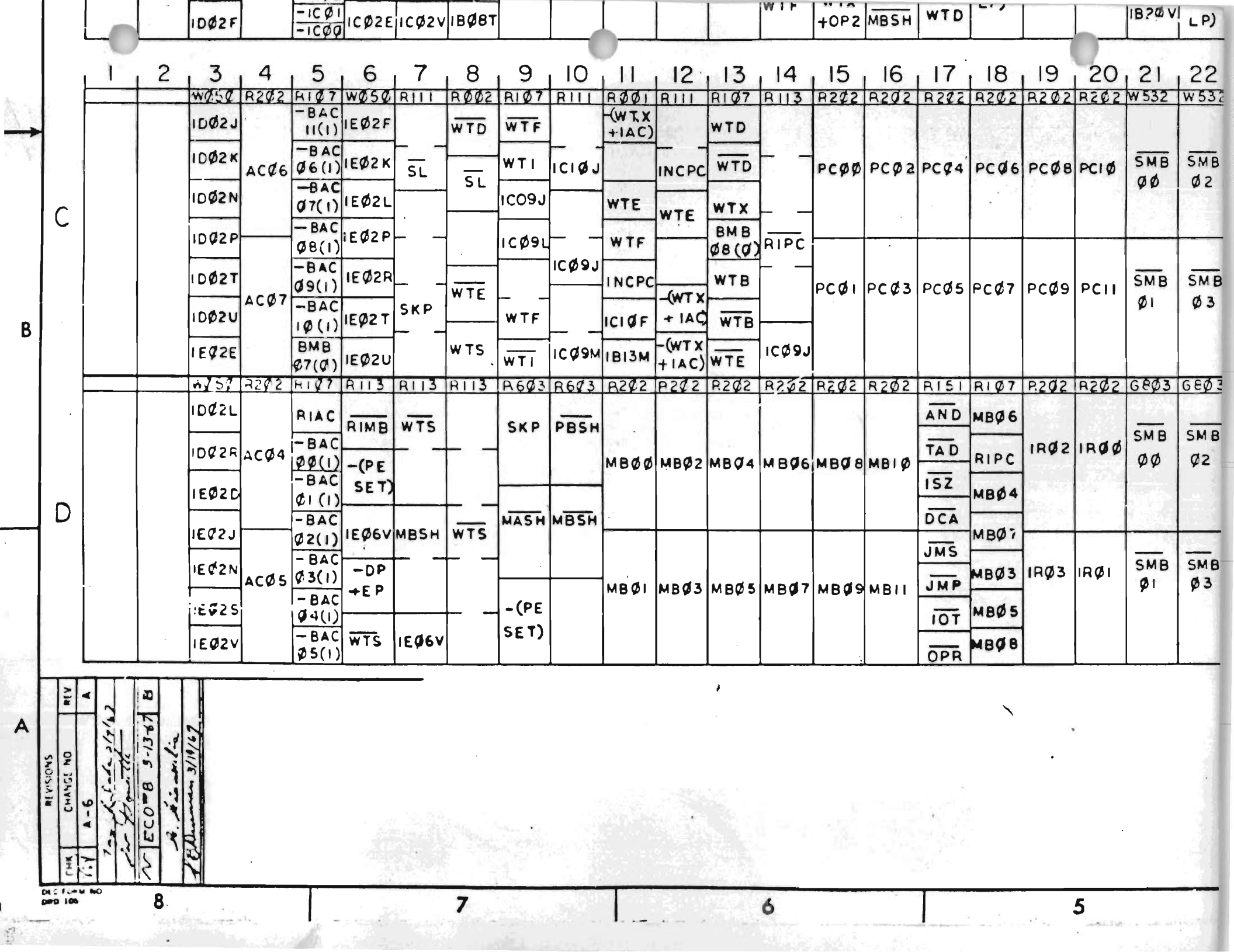
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
			WØ5Ø	R2Ø2	RIØ7	WØ5Ø	RIII	R00Ø2	RIØ7	RIII	R00I	RIII	RIØ7	RII3	R2Ø2	R2Ø2	R2Ø2	R2Ø2	R2Ø2	R2Ø2	W532	W5
C			IDØ2J	AC06	-BAC 11(1)	IEØ2F		WTD	WTF		-(WTX +IAC)		WTD									
			IDØ2K		-BAC Ø6(1)	IEØ2K	SL	SL	WTI	ICIØJ		INCPC	WTD		PCØØ	PCØ2	PCØ4	PCØ6	PCØ8	PCIØ	SMB ØØ	SMB Ø2
			IDØ2N		-BAC Ø7(1)	IEØ2L			ICO9J		WTE	WTE	WTX									
					-BAC								BMB									

→

24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
R107	R111	R113	R113	R6Ø2	R2Ø2	R2Ø2	R2Ø2	R2Ø2	RØØ1	R111	RØØ1	R3Ø2	R6Ø2	R111	RØ22	R107				
BTØØ		-BT ØØ-Ø1	-BT ØØ-11						TØ	$\overline{SY}$			-(SP +PCA)			ION				
SX	ION	-BT (ØØ)		$\overline{SL}$	TØ	T2	T4	T6	T1			OS		$\overline{PEC}$	$\overline{PEC}$	$\overline{SSK}$				
-BT ØØ-11	$\overline{SY}$								T2	RUN				IOP4		IOP1				
BT ØØ-Ø6		-BT (13)	$\overline{SY}$						T3		RUN					IOP2				
PEC				$\overline{RT}$	EX	T1	T3	T5	··4					IOP4						
$\overline{INT}$	$\overline{SY}$	-BT (12)							T5	$\overline{RIAC}$		OS		SAI	SAI	IOP1				
SY		WT X ROTP	IOP4						T6		SAI					IOP1				
R113	R113	RØØ2	R6Ø2	R2Ø2	R6Ø3	R6Ø3	R6Ø3	R4Ø1	RIØ7	R2Ø2	R2Ø2	R113	RIØ7	R6Ø3	W328	WØØ5				
	$\overline{SY}$	$\overline{SY}$			-A ØØ-Ø1	-A13	-A ØØ-11		-(EX +DC)			EX TDC	IOP4	$\overline{LP}$	BAC 9-11 IOP 1,2,4 PWR CLEAR	S				
$\overline{C}$		$\overline{RL}$	$\overline{LSH}$	ZI					$\overline{ACSH}$		LD	$\overline{SSK}$	BMB Ø3 (1)			-INT				
					-A ØØ	LSH	RUN	$\overline{CLK}$	$\overline{ACSH}$				BMB Ø3 (Ø)			S				
$\overline{ACSH}$	$\overline{SX}$								$\overline{SSK}$			$\overline{SSK}$	BMB Ø4 (1)	$\overline{EP}$		S				
																S				
																WTS				
																MBII				
L		$\overline{SY}$	$\overline{RL}$	CA	-[A (ØØ-11) +A(12)]	-A12	-A		BTI2	RUN	DC	$\overline{TP}$	BMB Ø4(Ø)			-INT				
									-(DP +EP)				BMB Ø5 (1)	$\overline{DP}$		-SKP				
-(DP +EP)	$\overline{C}$	$\overline{SAC}$							INHIB 1			IOP4	BMB Ø5 (1)			IOP4				
																IOP2				
																IOP1				
																-C				

24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
G6Ø8	W532	W532	W532	W532	R2Ø2	WØØ5	R2Ø2		G6Ø8	WIØ8	WIØ8	R2Ø2	R6Ø3	R6Ø2	W5Ø1	W5Ø6				
						-SMB			$\overline{MBØØ}$											

D A B C


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
A B C D
IDØ2F -ICØ1 -ICØØ ICØ2E ICØ2V IBØ8T WTF +OP2 MBSH WTD IB?Ø V LP)
WØ5Ø R2Ø2 R1Ø7 WØ5Ø R111 RØØ2 R1Ø7 R111 RØØ1 R111 R1Ø7 R113 R2Ø2 R2Ø2 R2Ø2 R2Ø2 R2Ø2 W532 W532
IDØ2J IDØ2K IDØ2N IDØ2P IDØ2T IDØ2U IEØ2E ACØ6 ACØ7 -BAC 11(1) -BAC Ø6(1) -BAC Ø7(1) -BAC Ø8(1) -BAC Ø9(1) -BAC 1Ø(1) BMB Ø7(Ø) IEØ2F IEØ2K IEØ2L IEØ2P IEØ2R IEØ2T IEØ2U SL SL SKP WTD WTE WTS WTF WTI ICØ9J WTF WTI ICIØJ ICØ9L ICØ9J ICØ9M -(WTX +IAC) WTE WTF INCPC ICIØF IBI3M -(WTX +IAC) -(WTX +IAC) INCPC WTE WTD WTD WTX BMB Ø8(Ø) WTB WTB WTE RIPC ICØ9J PCØØ PCØ1 PCØ2 PCØ3 PCØ4 PCØ5 PCØ6 PCØ7 PCØ8 PCØ9 PCIØ PCI1 SMB ØØ SMB Ø1 SMB Ø2 SMB Ø3
WØ5Ø R2Ø2 R1Ø7 R113 R113 R113 R6Ø3 R6Ø3 R2Ø2 R2Ø2 R2Ø2 R2Ø2 R2Ø2 R2Ø2 R151 R1Ø7 R2Ø2 R2Ø2 GEØ3 GEØ3
IDØ2L IDØ2R IEØ2D IEØ2J IEØ2N IEØ2S IEØ2V ACØ4 ACØ5 RIAC -BAC ØØ(1) -BAC Ø1(1) -BAC Ø2(1) -BAC Ø3(1) -BAC Ø4(1) -BAC Ø5(1) RIMB -(PE SET) IEØ6V -DP +EP WTS IEØ6V WTS MBSH WTS SKP MASH -(PE SET) PBSH MBSH MBØØ MBØ1 MBØ2 MBØ3 MBØ4 MBØ5 MBØ6 MBØ7 MBØ8 MBØ9 MBIØ MBI1 AND TAD ISZ DCA JMS JMP IOT OPR RIPC MBØ6 MBØ4 MBØ7 MBØ3 MBØ5 MBØ8 IRØØ IRØ1 IRØ2 IRØ3 SMB ØØ SMB Ø1 SMB Ø2 SMB Ø3
REVISIONS
REV A
CHANGE NO A-6
CHK
ECO#8 5-13-62 B
8 7 6 5

-(DP +EP)	$\overline{C}$	$\overline{SAC}$	$\overline{RL}$	CA	-LA (00-11) +A(12)	-A12	-A		-(DP +EP) INHIB 1	RUN	DC	IOP4	BMB 05 (1) BMB 05 (1)	$\overline{DP}$		IOP4 IOP2 IOP1 -C

Slot	Module (C)	Signals (C)	Module (D)	Signals (D)
23	...2	...IB; ...B 5	...03	...B; ...B
24	G608	SMB 00 TO SMB 11		MPS
25	W532	SMB 06; SMB 07	G803	SMB 06; SMB 07
26	W532	SMB 08; SMB 09	G803	SMB 08; SMB 09
27	W532	SMB 10; SMB 11	G803	SMB 10; SMB 11
28	W532	MPS	G803	MPS
29	R202	C; D	R202	E; F
30	W005	-SMB 00 TO -SMB 11; -MPS; -RAC		
31	R202	PIR		
32				
33	G608	MB00 TO MB11; INHIB 1; INHIB 2; PBB		READ; WRITE
34	W108	M300; MB01; MB02; MB03; M304		MB05; MB06; MB07; INHIB 1; INHIB 2
35	W108	MB08; MB09; MB10; MB11; PBB		READ; WRITE; INHIB 2
36	R202	A; B	R111	STRB; STRB; DONE; DONE; IOP1; IOP1
37	R603	CMB; -SP+ PCP+ LP+ A00+ WTB; CP	R302	SP1; SP2
38	R602	SP4; AI2 (EX+ DC+ LD)	R202	ION; WTF
39	W501	TP	R002	IF40K; IF40K; DONE; STRB
40	W506	MPC; PPC	W028	BMB 6-11
41				
42				
43				
44				

C

D

B

ISSUED APR 7 1967

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	DRN R. L. Perier DATE 12/12/66		digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
	CHK'D. DATE 12-15-66		TITLE MODULE UTILIZATION (A-D) (4K)
	ENG. DATE 12-16-66		
	PROJ. ENG. DATE 12-16-66		
	PROD. DATE 12-16-66		
MATERIAL	FIRST USED ON D-UA-8S-0-0		SIZE D CODE MU NUMBER 8S-0-26 REV. B
FINISH	SCALE		
	SHEET 1 OF 2		DIST.

A

SIZE D CODE MU NUMBER 8S-0-26 REV B

4 3 2 1

8 | 7 | 6

D

E

Slot	Module	Signals
1		
2		
3	RØØ1	ACØØ, ACØ1, ACØ2, ACØ3, ACØ4, PG, PE
4	R2Ø2	ACØ2, ACØ3
5	WØ5Ø	IFØ2[illegible], IFØ2S, *, *, *, *, *
6	R2Ø2	PT, PE
7	WØ5Ø	*, IFØ2R, IFØ2T, IFØ2V, *
8	WØØ5	-IAC, -IAC1[illegible], -IACØ9, -IACØ7, -ACSH, -IACØ8, SKS, -IACØ6, -IACØ5, -IACØ4, -IACØ3, -IACØ2, -IACØ1, -IACØØ, -ASCH
9	R113	ROTR, ROTL, IF15T, AI* IR3, -AI* IR3
10	R113	OP1, I/O CLR, IF19H, IE1ØV
11	R113	OP2, OPT IOT, IF15F, -SP, ISZ* Z1
12	R2Ø2	PGZ, WTS
13	R113	RIMA, PGZ, CLL, CML
14	R113	RIVA
15	R2Ø2	MA ØØ, MA Ø1
16	R2Ø2	MA Ø2, MA Ø3
17	R2Ø2	MA Ø4, MA Ø5
18	R2Ø2	MA Ø6, MA Ø7
19	R2Ø2	MA Ø8, MA Ø9
20	R2Ø2	MA 1Ø, MA 11
21	A7Ø2	-1ØV REF POW SUP
22	W1Ø8	VA[illegible] CE[illegible] TO MA Ø8

F

C

Slot	Module	Signals
1		
2		
3	R2Ø2	L, SKP
4	R2Ø2	ACØØ, ACØ1
5	R2Ø2	PG, PB
6	RØØ1	L, PB1-, L, SL, IFØ2T, IFØ7N, RIAC
7	R111	TP, IFØ7N, SKP
8	R111	L, SL, SKP, MBØØ
9	R111	SKP, MBØØ, RIAC, ACSH
10	R1Ø7	L, PBB, MAØ1, MAØ3, MAØØ, MAØ2, MA11
11	R1Ø7	MBØ2, MBØ3, MBØ4, MBØ5, MBØ7, MBØ8, MBØ9
12	R1Ø7	MBØØ, MBØ1, MBØ2, MBØ9, MB1Ø, MBØØ, MBØ1
13	R1Ø7	ROTR, MB13, -AI* IRS, MB1Ø, AI* IR3, -(OP IOT), MA 11
14	R113	IAC, CMA, IAC + CMA, RIAC
15	R111	RIMA, IF15P, IF15V
16	RØØ1	ROTR, ROTL, TP, IF17V, IF15P, IF15V
17	R111	ROTR, ROTL, IF17V
18	R1Ø7	MBØ5, SKP, OP1, WTE, OP2, I/O CLR, IF18T
19	R1Ø7	I/O CLR, IF19F, OPR, IF19L, CLL, CML, -(IAC + CMA)
20	R1Ø7	AND, TAD, ISZ, DCA, JMS, JMP, IOT
21		
22		

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
Ø8	G609									G609	WIØ8	WIØ8	R113	WØ28	WØ28	WØ28	WØ28				
										-MA ØØ -MA Ø3Ø	-MA 73Ø	-MA ØØ	START R/W CYCLE	IC	IC	BAC,	BMB				
										-MA Ø1 MA Ø31	MA Ø31	-MA Ø1	STRB ENAB READ	9-11 SKP	Ø-8	Ø-8	Ø-5				
										-MA Ø2 MA Ø4Ø	MA Ø4Ø	-MA Ø2	WHIB WRITE	INT CLA							
A	MA		M	E	M	O	R	Y													
O	ØØ1 MA									MA ØØ1 MA Ø41	MA Ø41	MA ØØ1	R401	R602	R602	R602	A111				
A	Ø61 TO		S	T	A	C	K							IOP1	IOP2	IOP4	WTF				
91	MA ØEØ MA Ø91									MA ØØ1 MA Ø5Ø	MA Ø5Ø	MA Ø11	-TSH				PIR				
										MA Ø51 MA Ø21	MA Ø51	MA Ø21		MR	START R/W CYCLE	START C/W CYCLE	SP4				

23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44

D E F C

FIND NO	MECHANICAL DESCRIPTION	PART NO.	DEPT. USAGE PROD	CUST	F/C
1	TABLE MODEL PDP-8S	D-UA-8S-0-0			
	TABLE MODEL PDP-8S (P.L.)	A-PL-8S-0-0			
	GUIDE, TOP COVER	B-MD-7405405-0-0			
	SHIELD, FILTER CIRCUIT	C-MD-7405569-0-0			
	SIDE BRKT, SHROUD	B-MD-7405402-0-0			
	SPACER, SHROUD	B-MD-7405401-0-0			
	COVER,BOTTOM	D-MD-7405404-0-0			
	AIR EXHAUST	D-MD-7405397-0-0			
	FOOT, REAR	B-MD-7405403-0-0			
	POSITIONING PLATE	B-MD-7405410-0-0			
	BEZEL CASTING REWORK	D-MD-7405414-0-0			
	SIDE POS. PLATE	A-MD-7406190-0-0			
2	TOP COVER	D-IA-7405409-0-0			
3	SWITCH BOARD ASSY	D-IA-5403836-0-0			
	SPACER#2 SWITCH BOARD	C-MD-5503902-0-0			
	ROCKER TO SWITCH	D-SC-7405229-8-0			
	ROCKER TO SWITCH	D-SC-7405229-9-0			
	ROCKER TO SWITCH	D-SC-7405229-6-0			
	SPACER#1 SWITCH BOARD	C-MD-5503839-0-0			
4	ETCH BOARD, SWITCHES	D-IA-5003838-0-0			
	EPOXY BOARD	1405020-0-0			
	PRINTED CIRCUIT LAYOUT	5003838-0-2			
5	CONTROL PANEL ASSY	D-AD-7005191-0-0			
	CONTROL PANEL ASSY (P.L.)	A-PL-7005191-0-0			
	SILK SCREEN-STEP#1(GRAY)	C-SS-7405621-0-0			
	SILK SCREEN-STEP#2(RUS.ORN)	C-SS-7405622-0-0			
	SILK SCREEN-STEP#3(BURNT ORN)	C-SS-7405623-0-0			
	SILK SCREEN-STEP#4(BLK)	C-SS-7405289-0-0			
	GLASS PANEL	D-MD-7005191-0-0			
6	INDICATOR LIGHT BOARD ASSY	D-IA-5403833-0-0			
7	ETCH BOARD LIGHTS(PDP-8S)	D-IA-5003835-0-0			
	EPOXY BOARD	1405019-0-0			
	PRINTED CIRCUIT LAYOUT	5003835-0-2			
8	GLASS SUPPORT	D-IA-7405412-0-0			
9	WIRING CASTING ASS'Y (4K)	D-AD-7005265-0-0			
	WIRING CASTING ASS'Y (4K)(P.L.)	A-PL-7005265-0-0			
	WIRING CASTING REWORK	E-MD-7405413-0-0			
	WIRED ASSY CASTING (C.P.)	A-CP-8S-0-31			
	WIRE LIST PDP-8S (8K)	K-WL-8S-0-21			
10	WIRING CASTING ASSY(8K)	D-AD-7005327-0-0			
	WIRING CASTING ASS'Y(8K)(P.L.)	A-PL-7005327-0-0			
	WIRING CASTING REWORK	E-MD-7405413-0-0			
	WIRED ASSY CASTING (C.P.).	A-CP-8S-0-31			
	WIRE LIST PDP-8S (8K)	K-WL-8S-0-21			
11	MTG BAR ASSY (10 CONN. BLOCKS)	D-AD-7005099-0-0			
	MTG BAR ASS'Y (10 CONN BLOCKS)	A-PL-7005099-0-0			
12	MTG BAR STD	D-AD-7005103-0-0			
	MTG BAR	D-MD-7405035-0-0			
13	CAPACITOR HOUSING ASSY	E-AD-7005190-0-0			
	CAPACITOR HOUSING ASS'Y (PL)	A-PL-7005180-0-0			
	JUMPER (BLK)	D-IA-7405360-2-0			
	JUMPER (BLK)	D-IA-7405360-4-0			
	JUMPER (RED)	D-IA-7405360-5-0			
	JUMPER (BLU)	D-IA-7405360-1-0			
	CONN WIRE (BLU)	D-IA-7405359-2-0			
	CONN WIRE (BLK)	D-IA-7405359-1-0			
	CONN WIRE (RED)	D-IA-7405359-3-0			
	CAP CONTAINER	D-MD-7405407-0-0			
	JUMPER (BLU)	D-IA-7405360-3-0			
14	CAP. HOLD-DOWN BRKT.	C-IA-7405406-0-0			

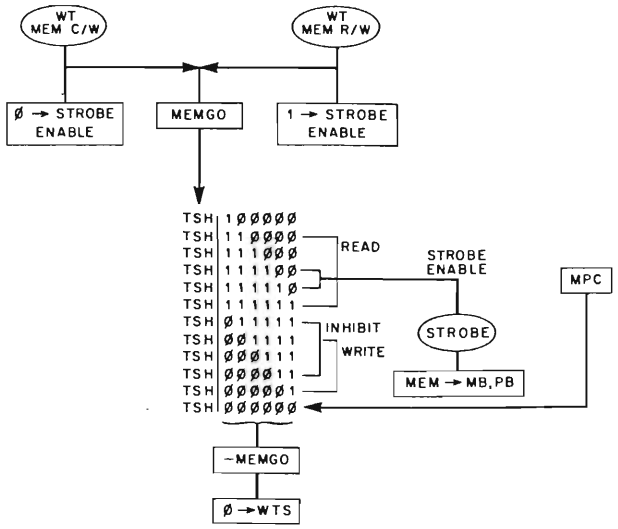
FIND NO	MECHANICAL DESCRIPTION	PART NO.	DEPT. USAGE PROD	CUST	F/C
15	REAR PANEL ASSY 50 & 60 CYCLE	D-AD-7005193-0-0			
	REAR PANEL ASSY 50 & 60 CYCLE	A-PL-7005193-0-0			
	SUPPORT GUSSET (L.H.)	C-MD-7405395-1-0			
	PIVOT BRKT	B-MD-7405393-0-0			
	TOP COVER STOP	B-MD-7405392-0-0			
	SUPPORT GUSSET (R.H.)	C-MD-7405395-2-0			
	FAN SCREEN	C-MD-7405389-0-0			
	MARG CHK SCOTCHCALS	C-SS-10801			
	PROTECTION COVER	B-MD-7404508-0-0			
	(TRANSFORMER CHK LABEL (50 CYCLES ONLY)	SS-100105-1			
	INPUT POWER LABEL (60 CYCLES)	SS-100104-1			
16	REAR PANEL	E-IA-7405396-0-0			
17	FAN MTG PLATE	C-IA-7405425-0-0			
18	COMPONENT MTG PLATE	D-IA-7405391-0-0			
19	SPACER, FAN	C-IA-7405426-0-0			
20	QUICK RELEASE MTG PLATE	C-IA-7405388-0-0			
21	SIDE SHROUD	D-IA-7405394-0-0			
	SIDE SHROUD(L.H.)	D-IA-7405394-1-0			
	SIDE SHROUD(R.H.)	D-IA-7405394-2-0			
22	AIR BAFFLE	E-IA-7405399-0-0			
23	MTG BRKT, REAR PANEL	C-IA-7405400-0-0			
24	POWER WIRING HARNESS	D-IA-7405648-0-0			
25	TELETYPE CONTROL PT08-A	D-UA-PT08-A-0			
	TELETYPE CONTROL PT08-A (PL)	A-PL-PT08-A-0			
	1943 MTG PANEL LABEL	SS-100153-1			
	LEFT END PANEL	C-MD-1943-0-1-0-2			
26	PT08 WIRED ASSEMBLY	D-AD-7005304-0-0			
	PT08 WIRED ASSEMBLY (PL)	A-PL-7005304-0-0			
	1943 FRAME CAST REWORK	C-MD-7405531-0-0			
27	CONN CABLE 8S-PT08	C-IA-7405600-1-0			
28	POWER CORD PT08-A TO PDP8S	C-AD-7005289-1-0			
	POWER CORD PT08-A TO PDP-8S (PL)	A-PL-7005289-0-0			
29	CABLE 4915 TO W070	D-AD-7005288-1-0			
	CABLE 4915 TO W070 (PL)	A-PL-7005288-0-0			
30	ASR TTY WITH PT08-A OPTION	D-AD-7005043-0-0			
	ASR TTY WITH PT08-A OPTION (PL)	A-PL-7005043-0-0			
	ASR 33 TELETYPE STAND (REWORK)	C-MD-7405529-0-0			
	PROTECTION PLATE ASR 33	1405292-0-0			
31	4K MEMORY	NO # AVAILABLE			
31	H281 MEMORY (8K)	D-SC-3005120-0-0			

DI-85-0-27
DWG IDX LST

DEPT. USAGE		
PROD	CUST	F/C

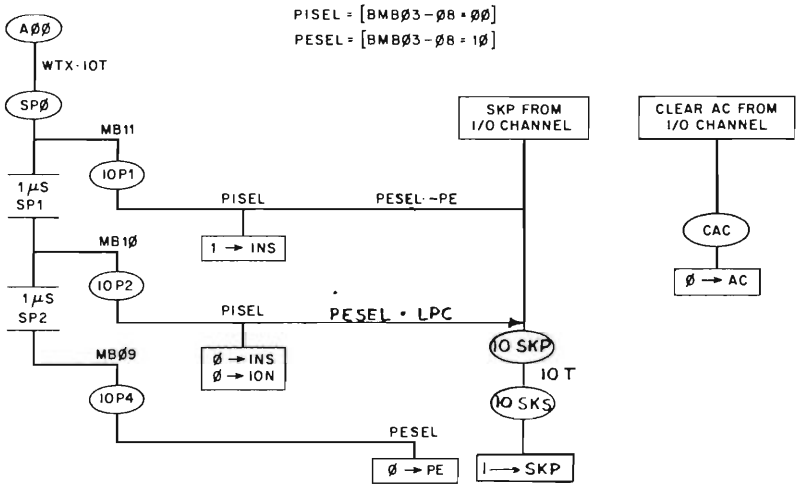
ELECTRICAL					
FIND NO	DESCRIPTION	PART NO.	PROD	CUST	F/C
1	TABLE MODEL PDP-8S(4K)	A-WL-8S-0			
	WIRING CASTING ASS'Y	D-AD-7005265-0-0			
	WIRING CASTING ASS'Y	A-PL-7005265-0-0			
	WIRE LIST PDP-8S	K-WL-8S-0-6			
	MEMORY BLOCK DIAGRAM	D-BS-8S-0-4			
	PDP8S BLOCK DIAGRAM	D-BD-8S-0-2			
	KEYS SWITCHES TIMING DIAGRAM	D-TD-8S-0-1			
	TIMING DIAGRAM	D-TD-8S-0-3			
	MB	D-BS-8S-0-9			
	ACCNT	D-BS-8S-0-10			
	BTG	D-BS-8S-0-11			
	MA	D-BS-8S-0-12			
	WORD TIME GEN.	D-BS-8S-0-13			
	ADDER	D-BS-8S-0-14			
	CONTROL	D-BS-8S-0-15			
	IR	D-BS-8S-0-16			
	I/O	D-BS-8S-0-17			
	MEMORY	D-BS-8S-0-18			
	P.C. REGISTER	D-BS-8S-0-19			
	ACCUMULATOR	D-BS-8S-0-20			
	IO CABLE SCHEDULES	D-CL-8S-0-5			
	MEMORY BLOCK MU(4K)	D-MU-8S-0-26			
	MEMORY BLOCK MU(4K)	A-PL-8S-0-26			
1	TABLE MODEL PDP-8S(8K)	A-WL-8S-0			
	WIRING CASTING ASSY	D-AD-7005327-0-0			
	WIRE LIST PDP-8S(8K)	K-WL-8S-0-21			
	MEMORY BLOCK DIAGRAM(8K)	D-BS-8S-0-23			
	PDP-8S BLOCK DIAGRAM	D-BD-8S-0-2			
	KEYS SWITCHES TIMING DIAGRAM	D-TD-8S-0-1			
	TIMING DIAGRAM	D-TD-8S-0-3			
	MB	D-BS-8S-0-9			
	ACCNT	D-BS-8S-0-10			
	BTG	D-BS-8S-0-11			
	MA	D-BS-8S-0-12			
	WORD TIME GEN	D-BS-8S-0-13			
	ADDER	D-BS-8S-0-14			
	CONTROL	D-BS-8S-0-15			
	IR	D-BS-8S-0-16			
	I/O	D-BS-8S-0-17			
	MEMORY (8K)	D-BS-8S-0-22			
	P.C. REGISTER	D-BS-8S-0-19			
	ACCUMULATOR	D-BS-8S-0-20			
	MEMORY BLOCK MU(8K)	D-MU-8S-0-25			
	MEMORY BLOCK MU(8K)	A-PL-8S-0-25			
	IO CABLE SCHEDULES				
	CABLE INTERFACE PDP-8/S	D-IC-8S-0-32			
15	REAR PANEL ASS'Y (SH 3 OF 3)	D-AD-7005193-0-0			
25	TELETYPE CONTROL PT08-A (MTG IN TELETYPE)	A-WL-PT08-A-0			
	TELETYPE CONTROL PT08 LOGIC	D-BS-PT08-A-1			
	MODULE LOCATION TYPE PT08	D-MU-PT08-A-2			
	MODULE LOCATION TYPE PT08	A-PL-PT08-A-2			
	WIRING LIST TYPE PT08	A-WL-PT08-A-3			
	PT08-A WIREO ASSEMBLY	C-AD-7005304-0-0			
	TELETYPE MOD (ASR-33)	D-IC-7605185-0-0			
31	4K MEMORY	NO # AVAILABLE			
31	H281 MEMORY (8K MEMORY)	D-SC-3005120-0-0			

MEMORY



IN-OUT

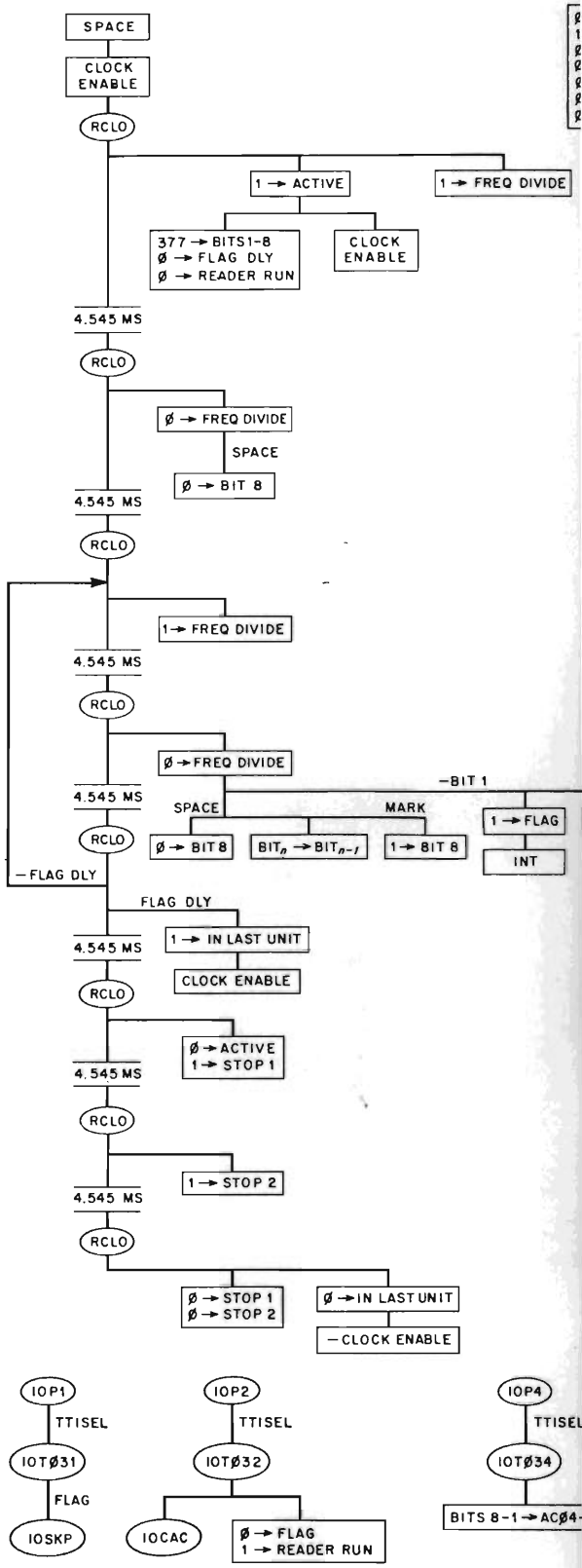
PISEL = [BMBØ3-Ø8 = ØØ]
PESEL = [BMBØ3-Ø8 = 1Ø]



TTI

TTISEL = [BMBØ3-Ø8 = Ø3]

When a key is struck or a tape line read, the distributor begins transmission with a 9.Ø9 ms start signal (space)



FD-85-0-29

MEM + IO FLOW

TTI

[BMBØ3 - Ø8 • Ø3]

he distributor begins transmission

I/O CLEAR

Ø → FLAG
1 → READER RUN
Ø → FREQ DIVIDE
Ø → ACTIVE
Ø → IN LAST UNIT
Ø → STOP 1
Ø → STOP 2

VE

1 → FREQ DIVIDE

CLOCK ENABLE

−BIT 1

MARK

1 → FLAG

1 → FLAG DLY

→ BIT 8

INT

Ø → IN LAST UNIT

−CLOCK ENABLE

IOP4

TTISEL

IOTØ34

BITS 8−1 → ACØ4-11

G
ADER RUN

TTO

TTOSEL • [BMBØ3-Ø8 • Ø4]

IOP1 — TTOSEL — IOTØ41 — FLAG — IOSKP

IOP2 — TTOSEL — IOTØ42 — Ø → FLAG

IOP4 — TTOSEL — IOTØ44 — BACØ4-11 → BITS 8-1, 1 → ENABLE

I/O CLEAR

Ø → FLAG
Ø → ACTIVE
Ø → FLAG DLY
Ø → BITS 1-8

If necessary wait until stop count is complete then wait for 22Ø Hz clock.

TCLO

ENABLE · −FLAG DLY · STOP 1 · STOP2

1 → ACTIVE

Ø → LINE

Transmit start signal (space)

4.545 MS

Transmission period 1 unit (space)

TCLO

1 → FREQ DIV

Ø → STOP 2

4.545 MS

TCLO

Ø → FREQ DIV

Ø → STOP 1

4.545 MS

ENABLE → BIT 8
$BIT_n \rightarrow BIT_{n-1}$

BIT 1 → LINE

Ø → ENABLE

Transmission period 1 unit

TCLO

Transmit bit (space or mark)

Note: when ENABLE and BITS 1-8 all clear, LINE = 1 so mark is transmitted.

−(BITS 1 - 8 • Ø)

4.545 MS

1 → FREQ DIV

BITS 1 - 8 • Ø

Ø → ACTIVE

1 → LINE

1 → FLAG

INT

1 → FLAG DLY

4.545 MS

TCLO

Ø → FLAG DLY
1 → STOP 2

Transmission period 2 units (2 marks) New IOTØ44 may occur after FLAG is set.

4.545 MS

TCLO

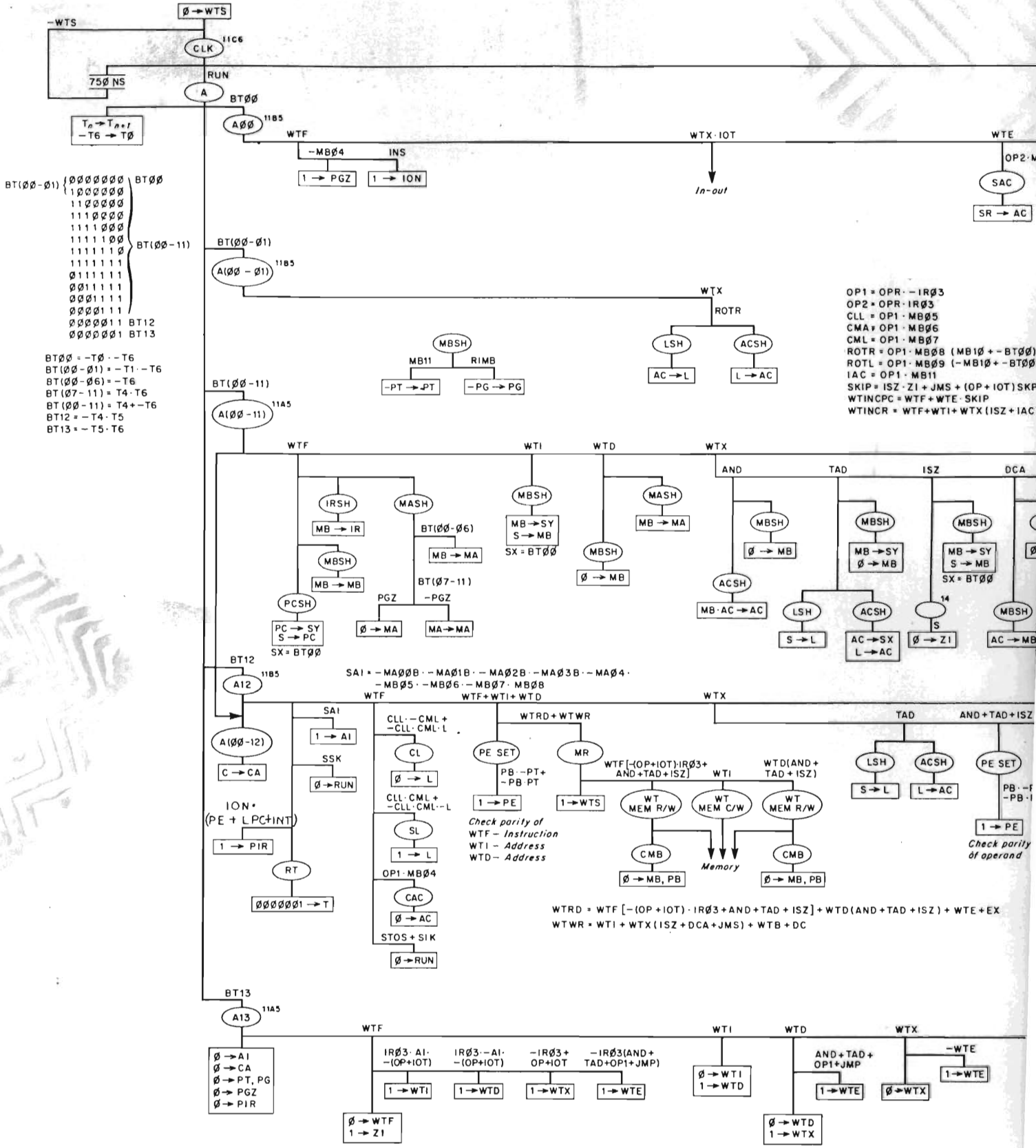
1 → STOP 1

4.545 MS

ENABLE

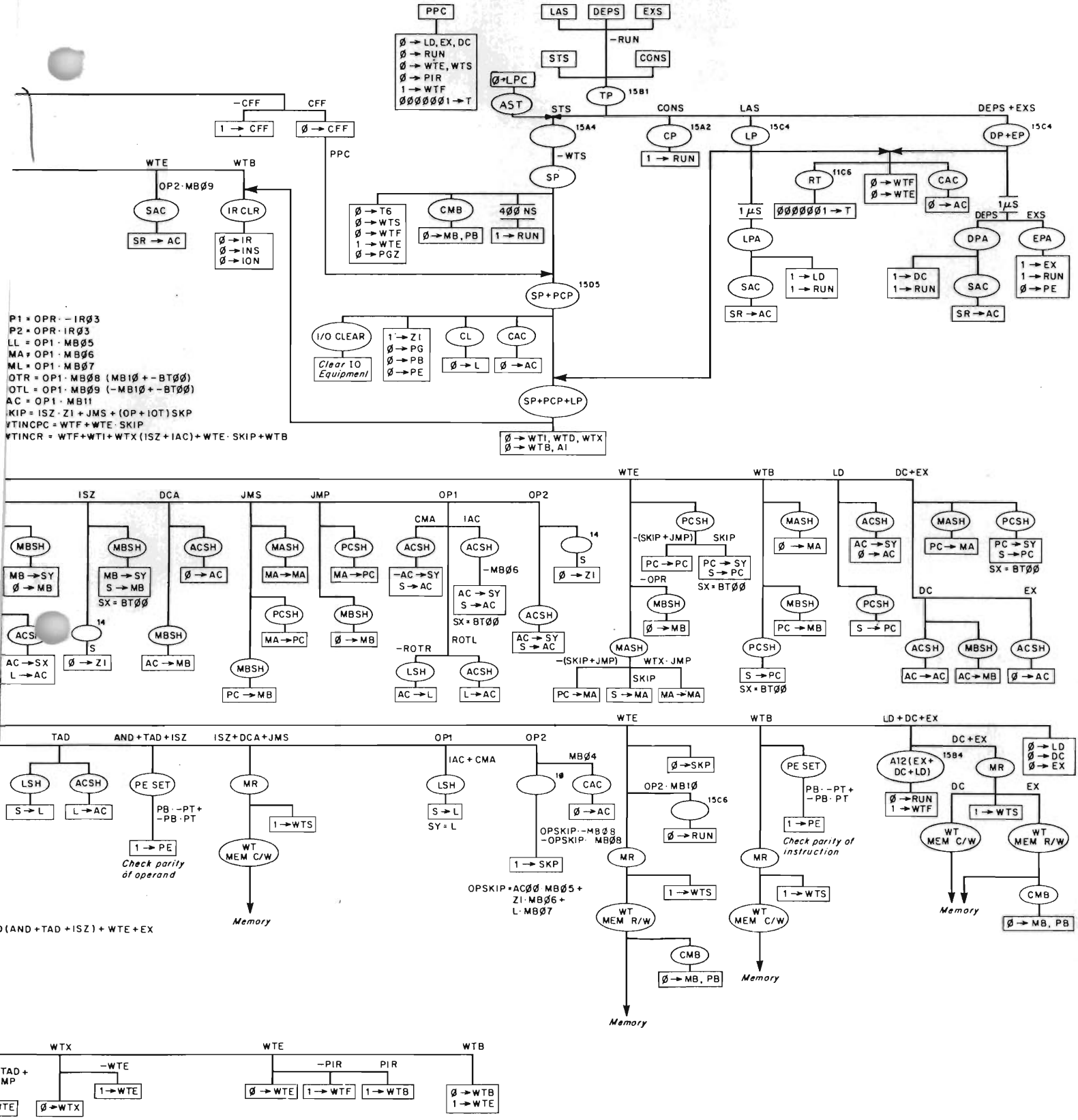
−ENABLE

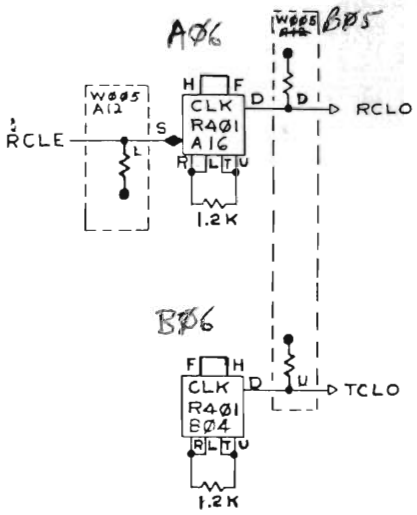
Continue marking line (LINE = 1)

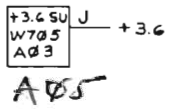


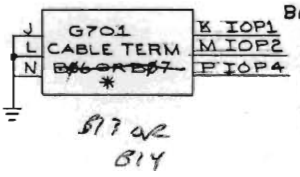
FD-85-0-30

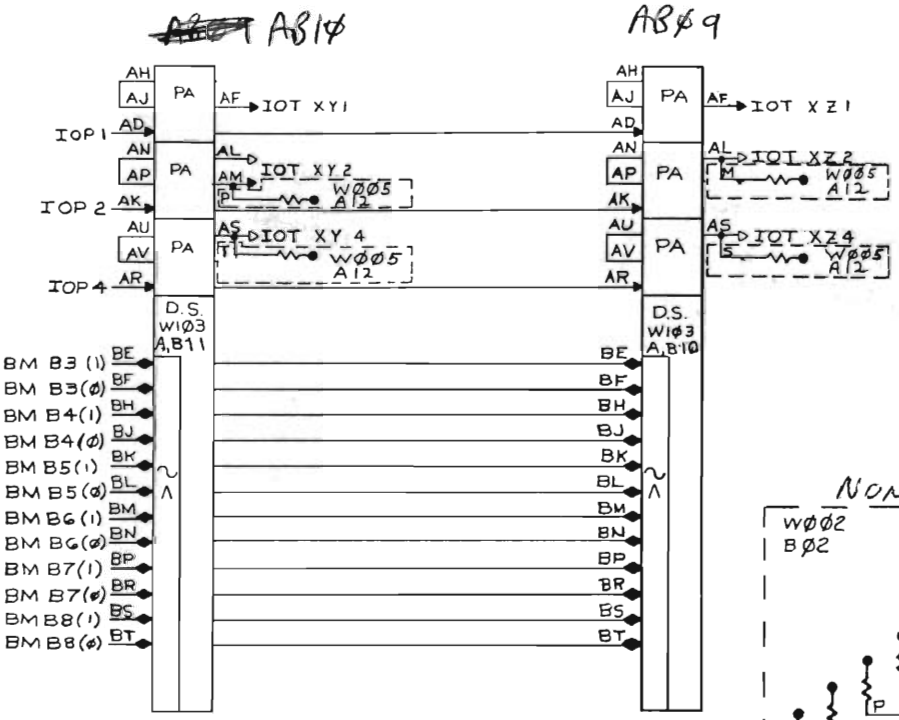
MAIN FLOW

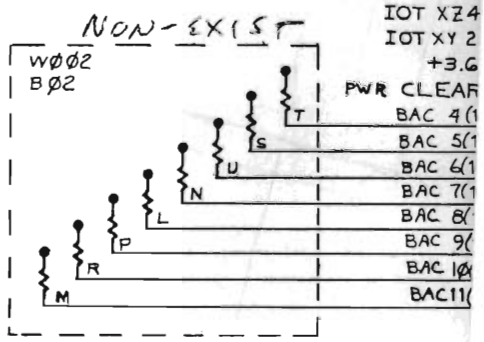

PPC
Ø → LD, EX, DC
Ø → RUN
Ø → WTE, WTS
Ø → PIR
1 → WTF
ØØØØØØ1 → T
LAS
DEPS
EXS
-RUN
STS
CONS
Ø→LPC
AST
TP 1581
-CFF
CFF
1 → CFF
Ø → CFF
PPC
STS 15A4
CONS 15A2
LAS 15C4
DEPS +EXS
DP+EP 15C4
-WTS
SP
CP 15A2
1 → RUN
LP 15C4
RT 11C6
ØØØØØØ1 → T
Ø → WTF
Ø → WTE
CAC
Ø → AC
1μS
DEPS
EXS
DPA
EPA
1 → DC
1 → RUN
SAC
SR → AC
1 → EX
1 → RUN
Ø → PE
WTE
WTB
OP2·MBØ9
SAC
SR → AC
IR CLR
Ø → IR
Ø → INS
Ø → ION
Ø → T6
Ø → WTS
Ø → WTF
1 → WTE
Ø → PGZ
CMB
Ø → MB, PB
4ØØ NS
1 → RUN
1μS
LPA
1 → LD
1 → RUN
SP+PCP 1505
I/O CLEAR
Clear IO Equipment
1 → ZI
Ø → PG
Ø → PB
Ø → PE
CL
Ø → L
CAC
Ø → AC
SP+PCP+LP
Ø → WTI, WTD, WTX
Ø → WTB, AI
P1 = OPR · -IRØ3
P2 = OPR · IRØ3
LL = OP1 · MBØ5
MA = OP1 · MBØ6
ML = OP1 · MBØ7
OTR = OP1 · MBØ8 (MB1Ø + -BTØØ)
OTL = OP1 · MBØ9 (-MB1Ø + -BTØØ)
AC = OP1 · MB11
SKIP = ISZ · ZI + JMS + (OP + IOT) SKP
WTINCPC = WTF + WTE · SKIP
WTINCR = WTF+WTI+WTX (ISZ + IAC) + WTE · SKIP + WTB
WTE
WTB
LD
DC+EX
ISZ
DCA
JMS
JMP
OP1
OP2
MBSH
MB → SY
Ø → MB
MBSH
MB → SY
S → MB
SX = BTØØ
ACSH
Ø → AC
MASH
MA → MA
PCSH
MA → PC
MBSH
Ø → MB
PCSH
MA → PC
MBSH
PC → MB
CMA
IAC
ACSH
-AC → SY
S → AC
ACSH
AC → SY
S → AC
SX = BTØØ
-MBØ6
ROTL
-ROTR
LSH
AC → L
ACSH
L → AC
14
S
Ø → ZI
ACSH
AC → SY
S → AC
PCSH
-(SKIP+JMP)
SKIP
PC → PC
PC → SY
S → PC
SX = BTØØ
-OPR
MBSH
Ø → MB
MASH
-(SKIP+JMP)
WTX · JMP
SKIP
PC → MA
S → MA
MA → MA
MASH
Ø → MA
MBSH
PC → MB
PCSH
S → PC
SX = BTØØ
ACSH
AC → SY
Ø → AC
MASH
PC → MA
PCSH
PC → SY
S → PC
SX = BTØØ
MBSH
PC → MB
PCSH
S → PC
DC
EX
ACSH
AC → AC
MBSH
AC → MB
ACSH
Ø → AC
TAD
AND+TAD+ISZ
ISZ+DCA+JMS
OP1
OP2
LSH
S → L
ACSH
L → AC
PE SET
PB: -PT+
-PB · PT
1 → PE
Check parity of operand
MR
1 → WTS
WT MEM C/W
Memory
IAC + CMA
LSH
S → L
SY = L
MBØ4
CAC
Ø → AC
OPSKIP · -MBØ8
-OPSKIP · MBØ8
1 → SKP
OPSKIP = ACØØ MBØ5 +
ZI · MBØ6 +
L · MBØ7
Ø → SKP
OP2 · MB1Ø
Ø → RUN
MR
1 → WTS
WT MEM R/W
CMB
Ø → MB, PB
Memory
PE SET
PB: -PT+
-PB · PT
1 → PE
Check parity of instruction
MR
1 → WTS
WT MEM C/W
Memory
LD + DC + EX
DC + EX
A12 (EX + DC + LD)
Ø → RUN
1 → WTF
MR
1 → WTS
Ø → LD
Ø → DC
Ø → EX
DC
EX
WT MEM C/W
WT MEM R/W
CMB
Ø → MB, PB
Memory
(AND + TAD + ISZ) + WTE + EX
WTX
-WTE
1 → WTE
Ø → WTX
WTE
-PIR
PIR
Ø → WTE
1 → WTF
1 → WTB
WTB
Ø → WTB
1 → WTE











IOT XY2
IOT XY1
+3.6
RCLO
IOT XY4
PWR CLEAR
TSO

IOT XZ2
IOT XZ1
TCLO
IOT XZ4
IOT XY 2
+3.6
PWR CLEAR
BAC 4(1
BAC 5(1
BAC 6(1
BAC 7(1
BAC 8(
BAC 9(
BAC 1Ø
BAC11(

** NOTE 3
DEVICE SELECTOR CODE CAN BE SELECTED BY THE PURCHASER FROM THE FOLLOWING POSSIBILITIES

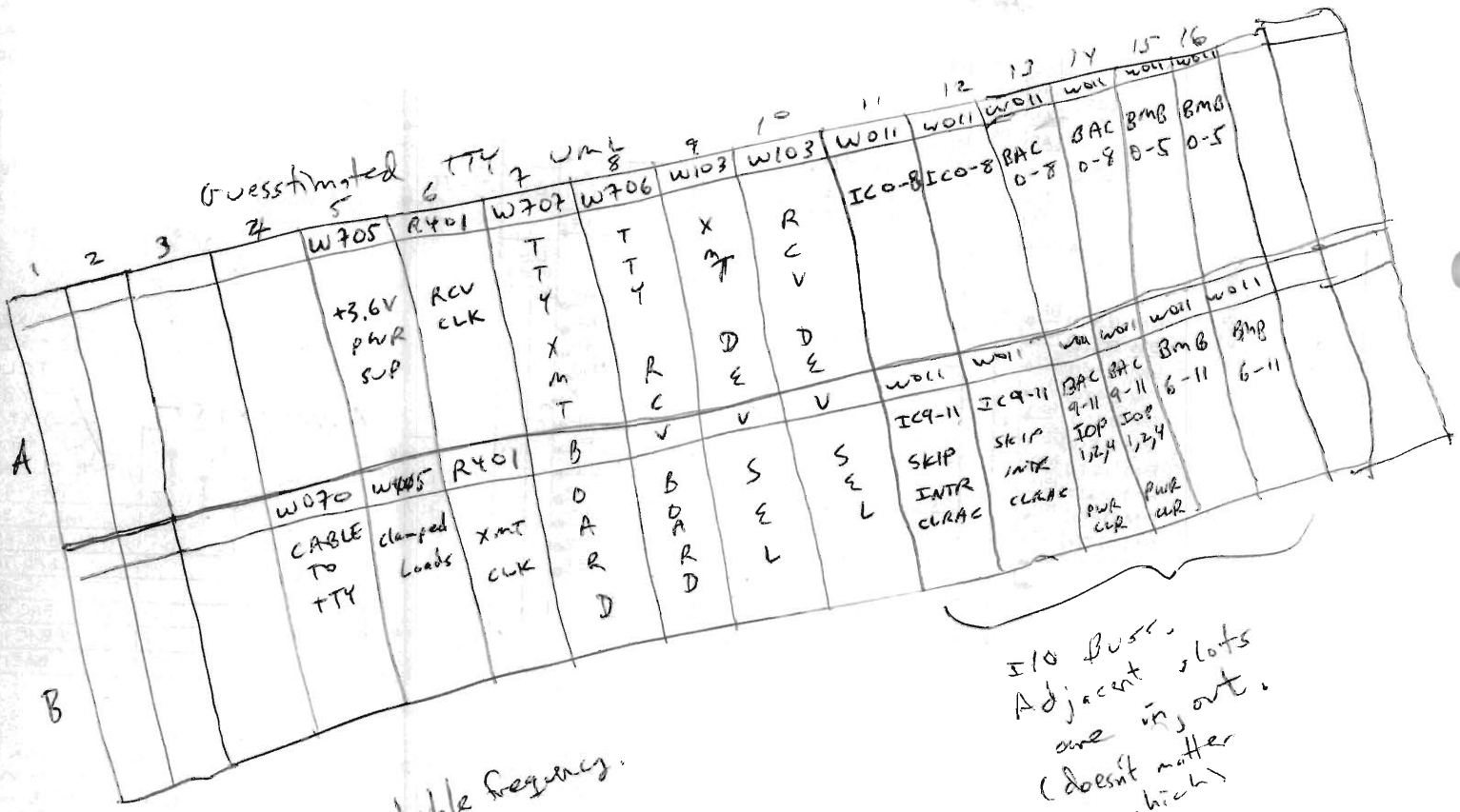
	RECVR XY	XMTR XZ	LINE
PDP-8 PDP-8/S	40	41	1
	42	43	2
	44	45	3
	46	47	4
	11	12	5
PDP8/S ONLY	03	04	1

* NOTE 2
THIS MODULE CAN H
DEPENDING ON WI
THE I/O CABLE HA
ON PDP-8 OR 8/S COMP
OTHER THAN THE
INSERTED IN THE
THE I/O CABLES IN
I/O BUS EXTENSIO

DEC FORM NO. DRD 102

PTO8 - A-1
TTY CTL

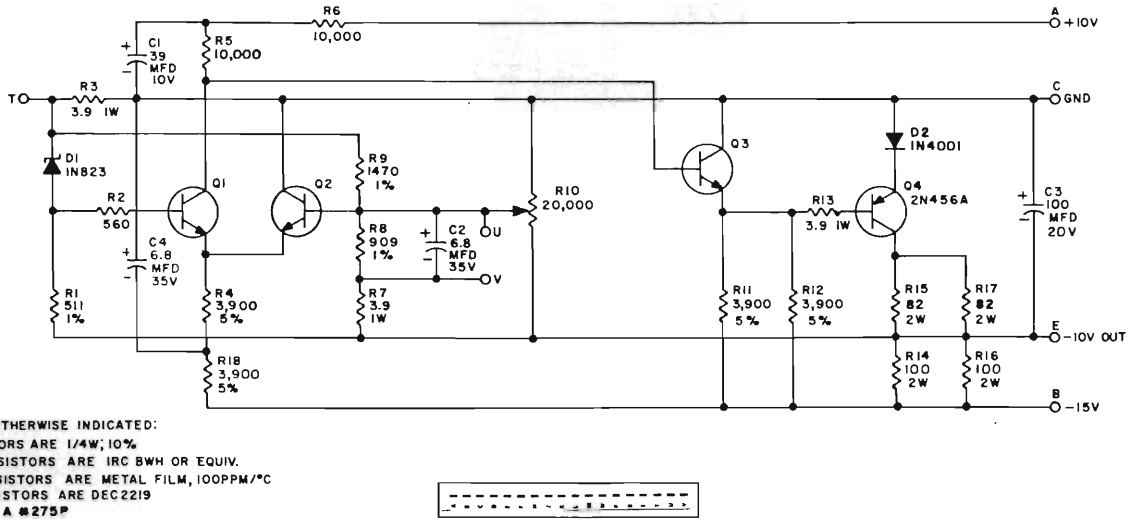
G701 Terminator
in B13 or B14



I10 Bus.
Adjacent slots
one in, out.
(doesn't matter
which)

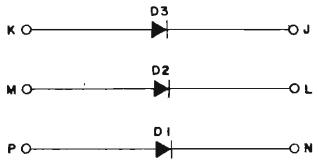
Clocks: double frequency.

S MODULE CAN HAVE EITHER LOCATION
PENDING ON WHICH OF THESE TWO SLOTS
E I/O CABLE HAS BEEN INSERTED.
PDP-8 OR 8/S COMPUTERS WITH OPTIONS
HER THAN THE PT08, THE G701 MUST BE
SERTED IN THE I/O DEVICE AT THE END OF
I/O CABLES IN THE CABLE SLOT THAT PROVIDES
BUS EXTENSION FOR IOP'S 1, 2, 4



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
3.9 RESISTORS ARE IRC BWH OR EQUIV.
1% RESISTORS ARE METAL FILM, 100PPM/°C
TRANSISTORS ARE DEC2219
R10 IS A #275P

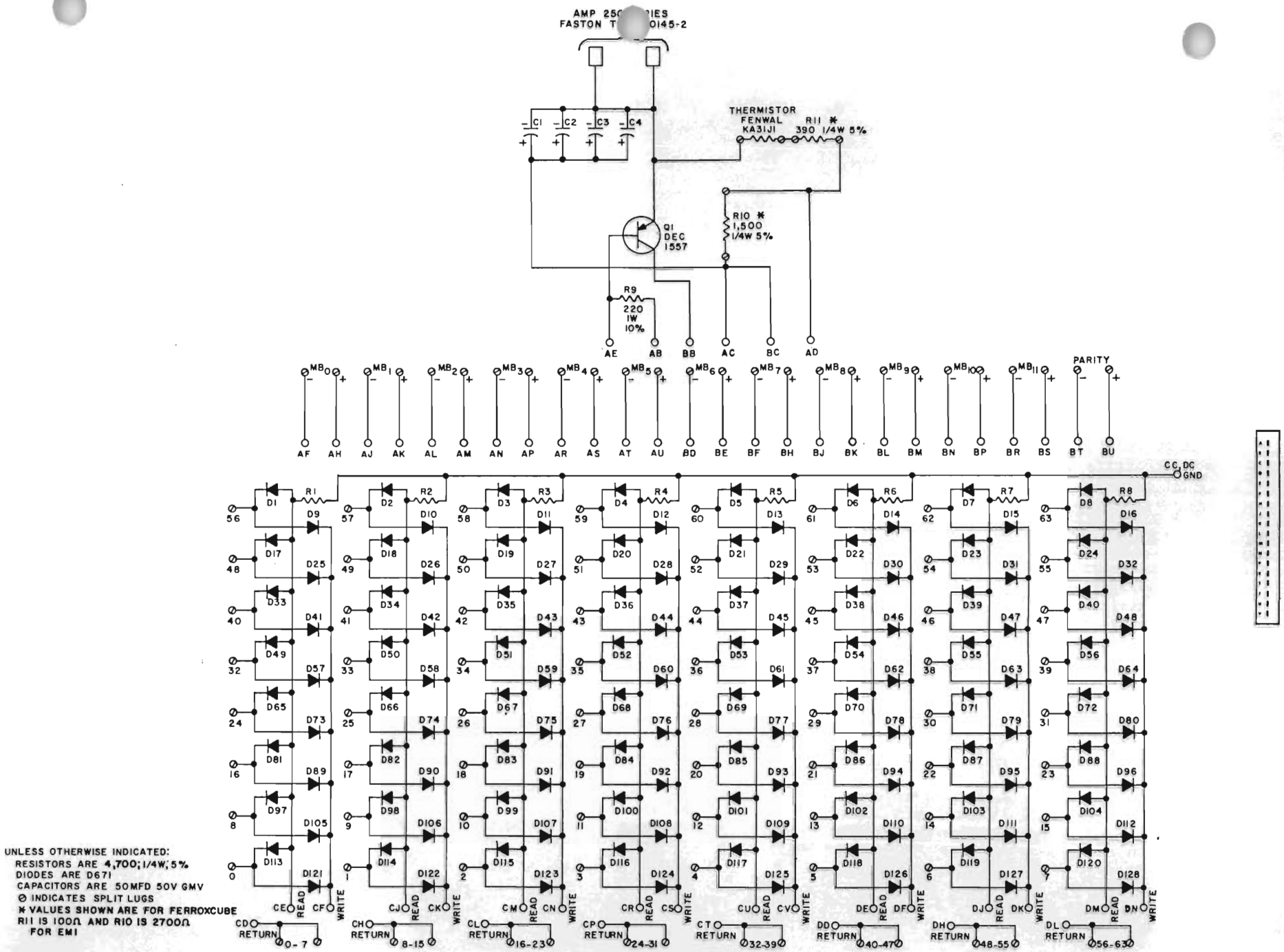
Reference Supply A702-0-1-B



UNLESS OTHERWISE INDICATED:
DIODES ARE D664

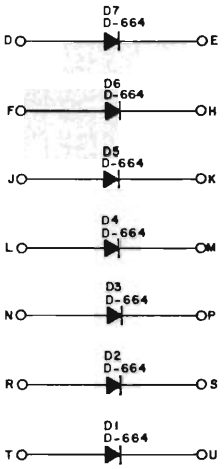
USE THE ETCH BOARD OF THE R001

Cable Terminator G701

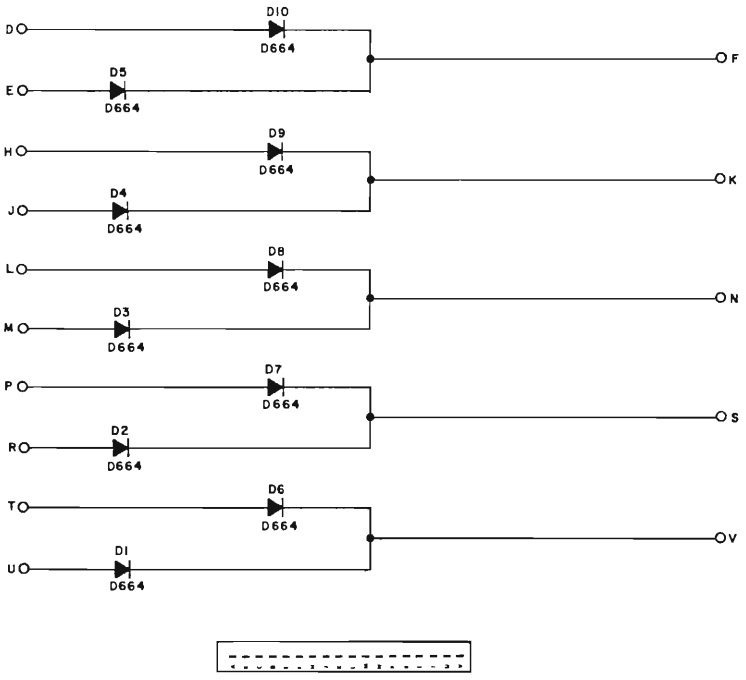


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 4,700; 1/4W; 5%
DIODES ARE D671
CAPACITORS ARE 50MFD 50V GMV
Ø INDICATES SPLIT LUGS
* VALUES SHOWN ARE FOR FERROXCUBE
R11 IS 100Ω AND R10 IS 2700Ω
FOR EMI

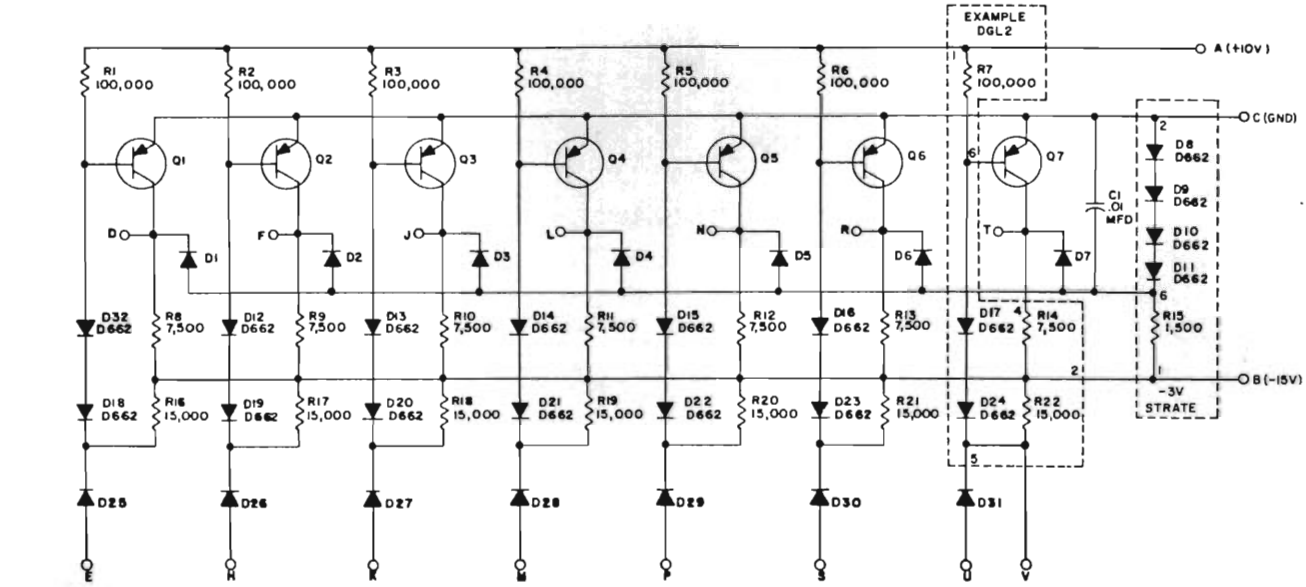
Memory Mounting Board G609



Diode R001-1

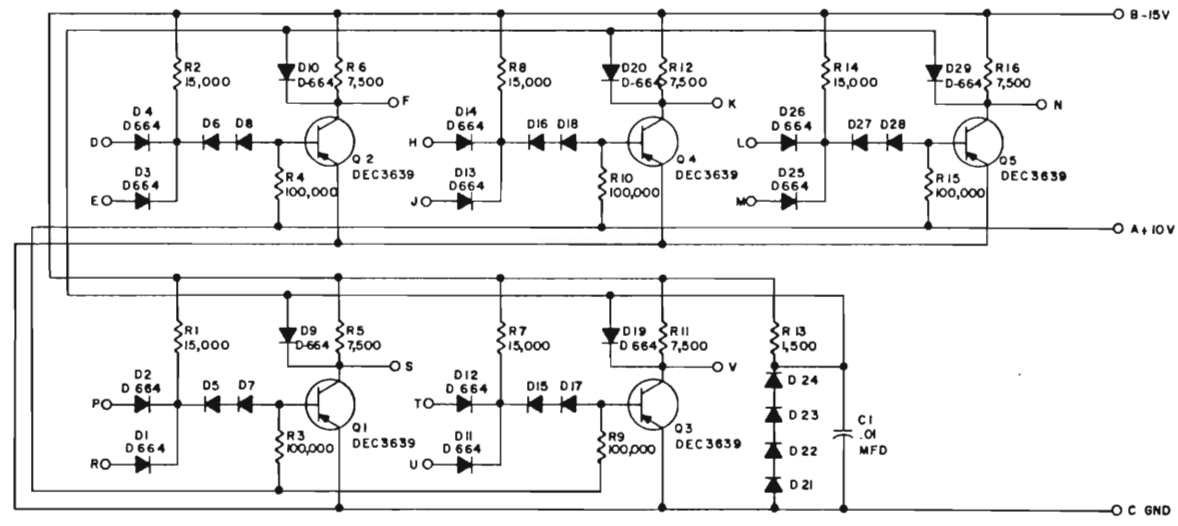


Diode R002-0-1-A



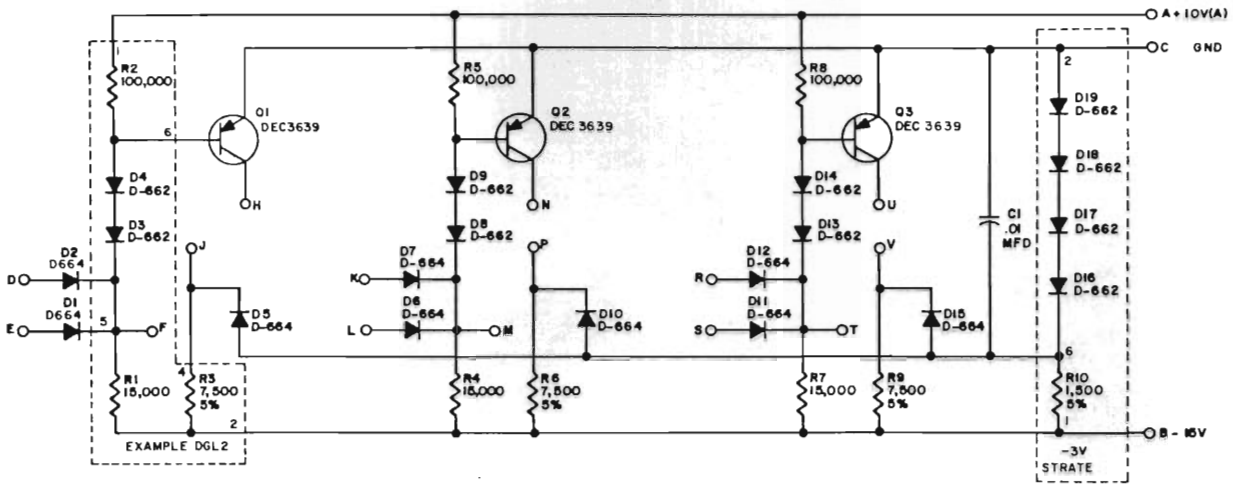
UNLESS OTHERWISE INDICATED;
RESISTORS ARE 1/4W, 5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIA

Inverter R107-0-1-E



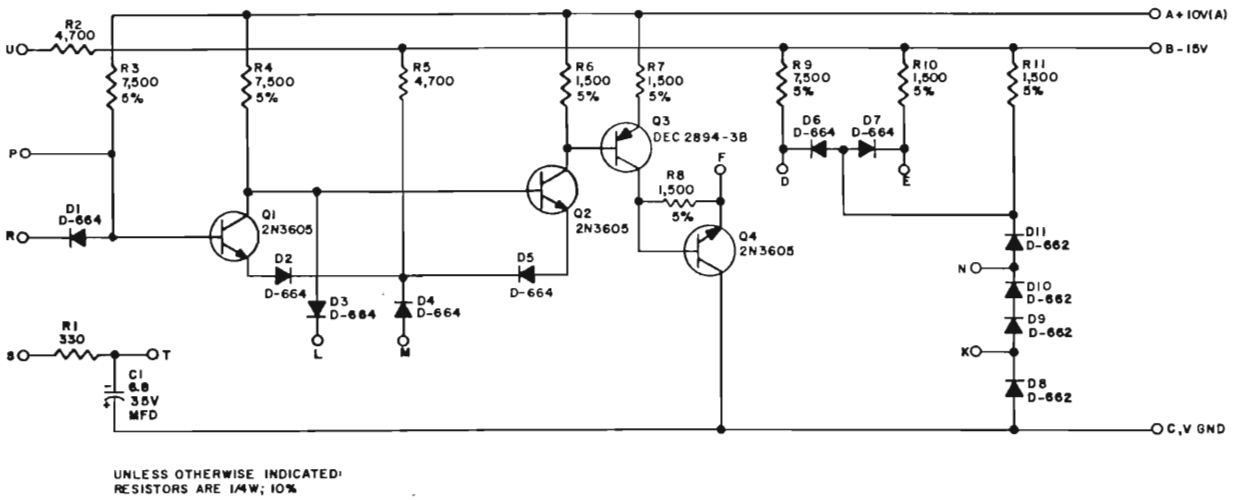
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 5%
DIODES ARE D 662

Diode Gate R113



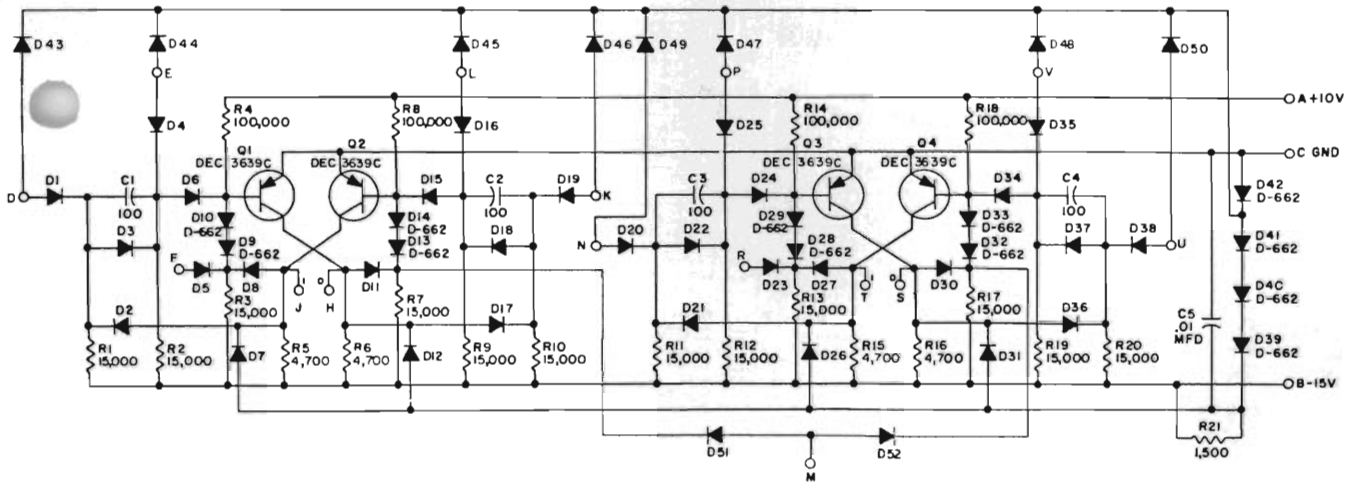
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIA

Diode Gate R111-0-1-E



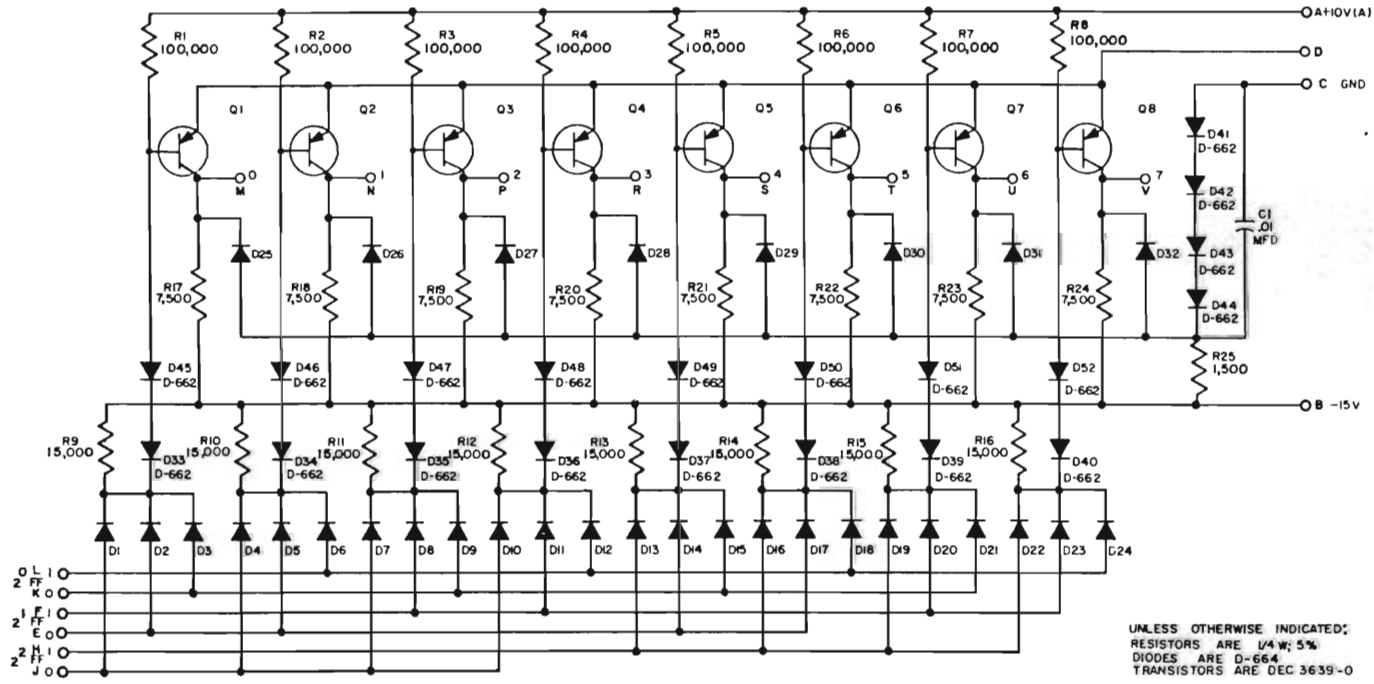
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%

Schmitt Trigger W501-5



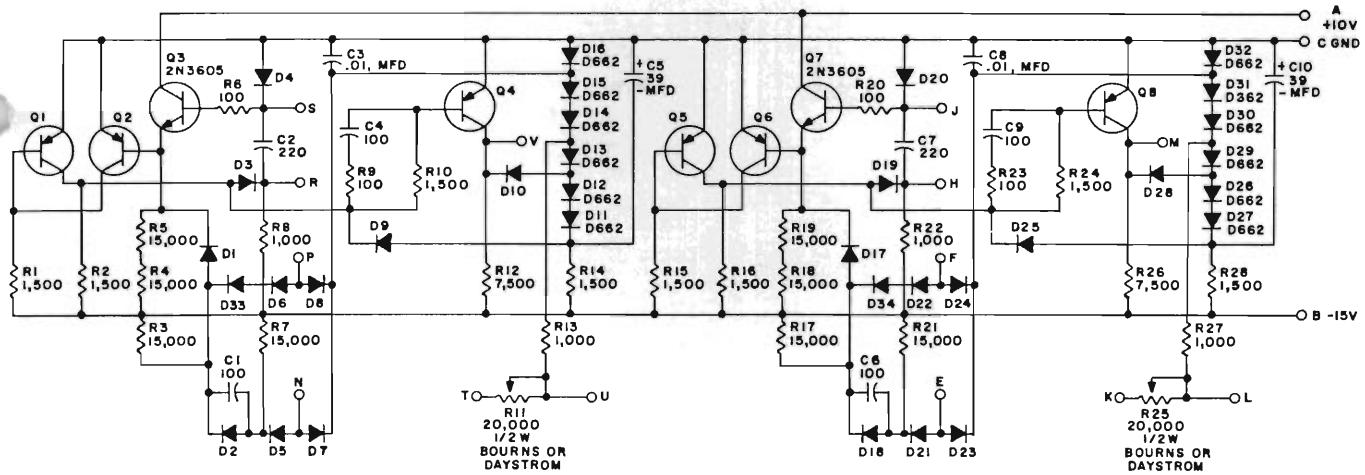
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

Dual Flip-flop R202-4



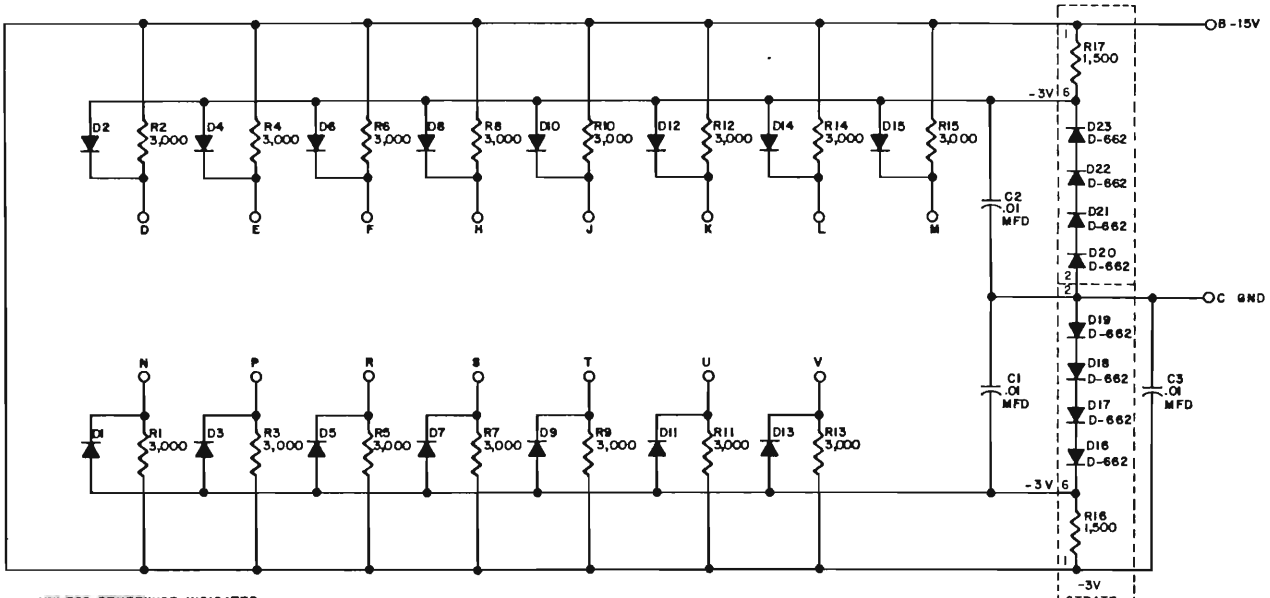
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639-0

Binary to Octal Decoder R151-3



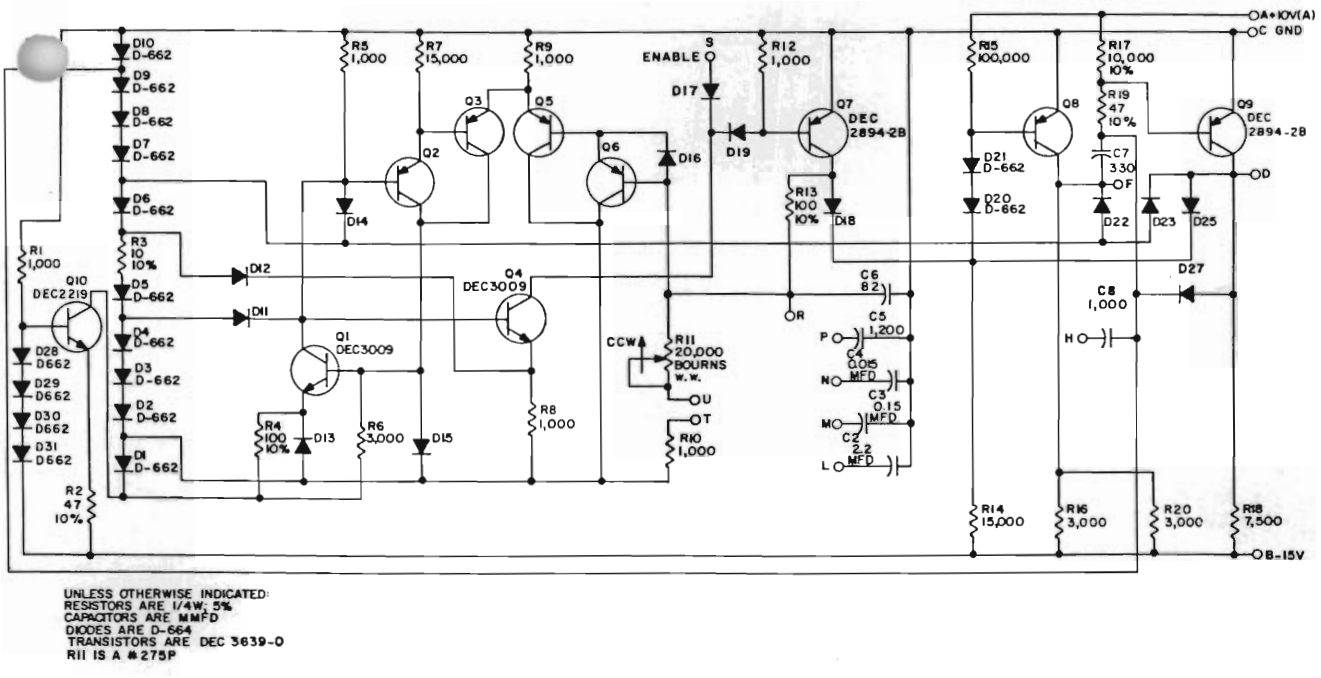
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D664
TRANSISTORS ARE DEC3639

Delay (one shot) R302-9

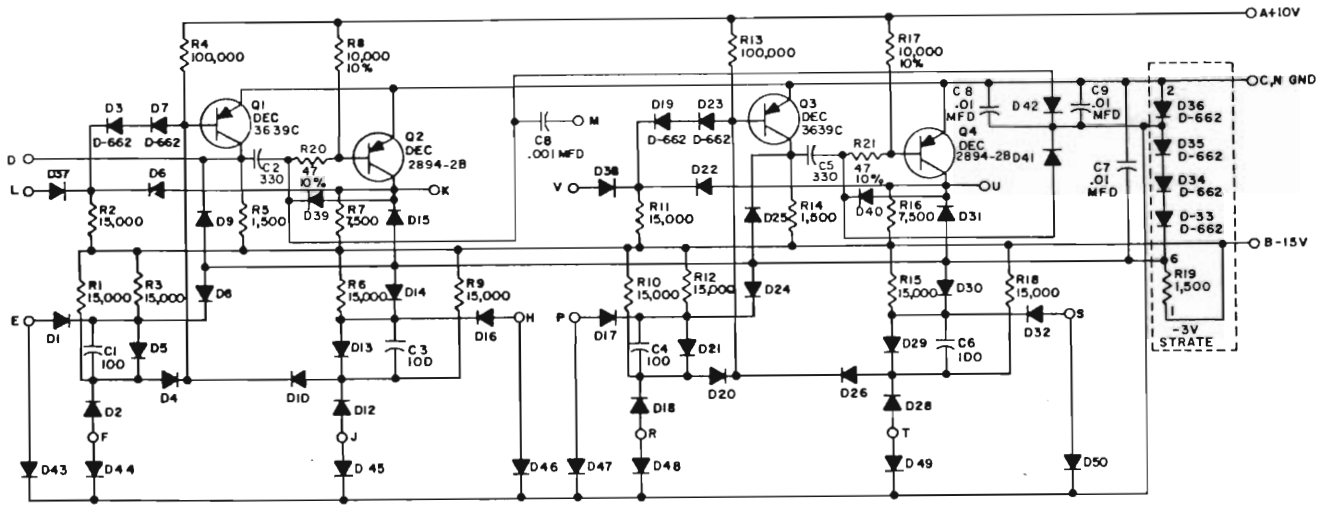


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D-664

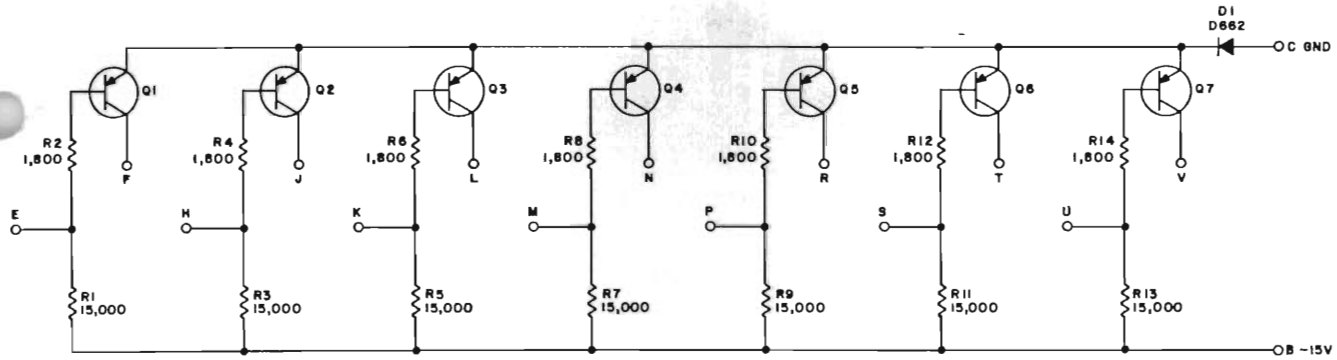
Clamped Loads W005-0-1-B



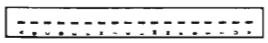
Clock R401-8



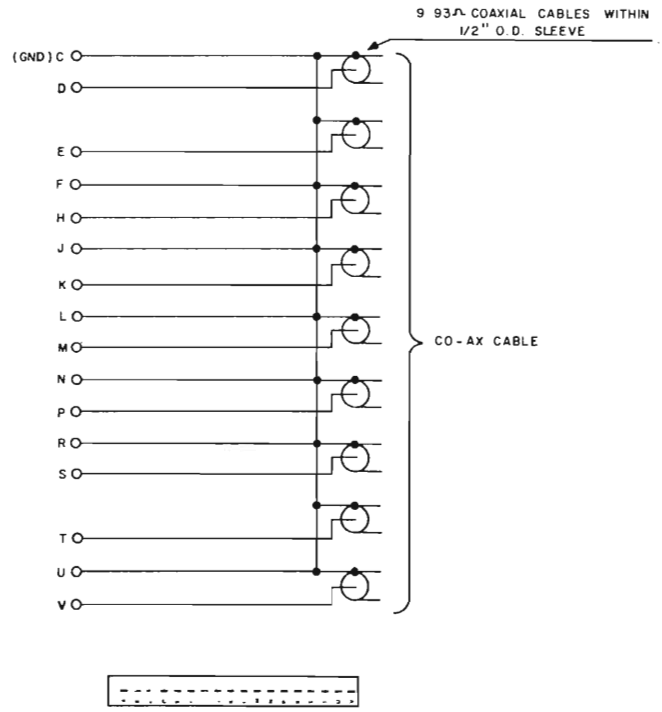
Pulse Amplifier R602-0-1-L



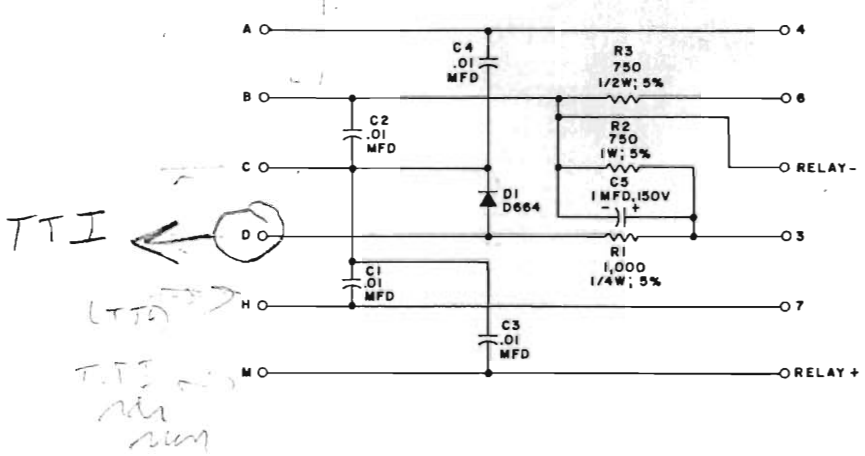
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
TRANSISTORS ARE DEC6534D (DEC6534B MAY BE SUBSTITUTED)



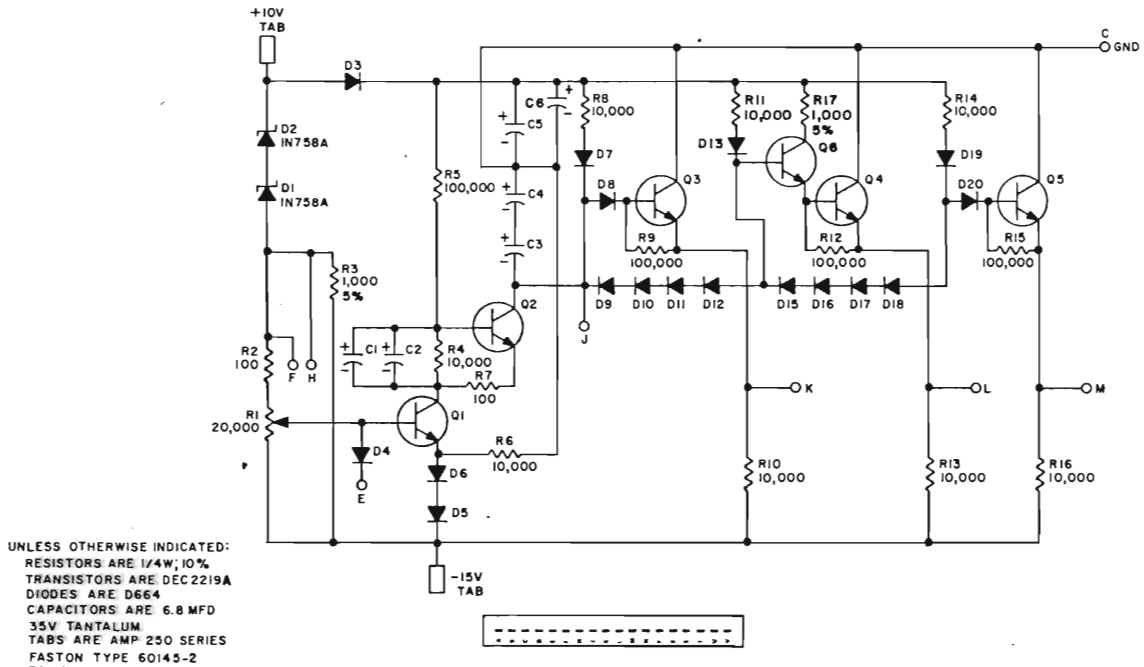
Indicator Driver W050-3



Signal Cable Terminator W011

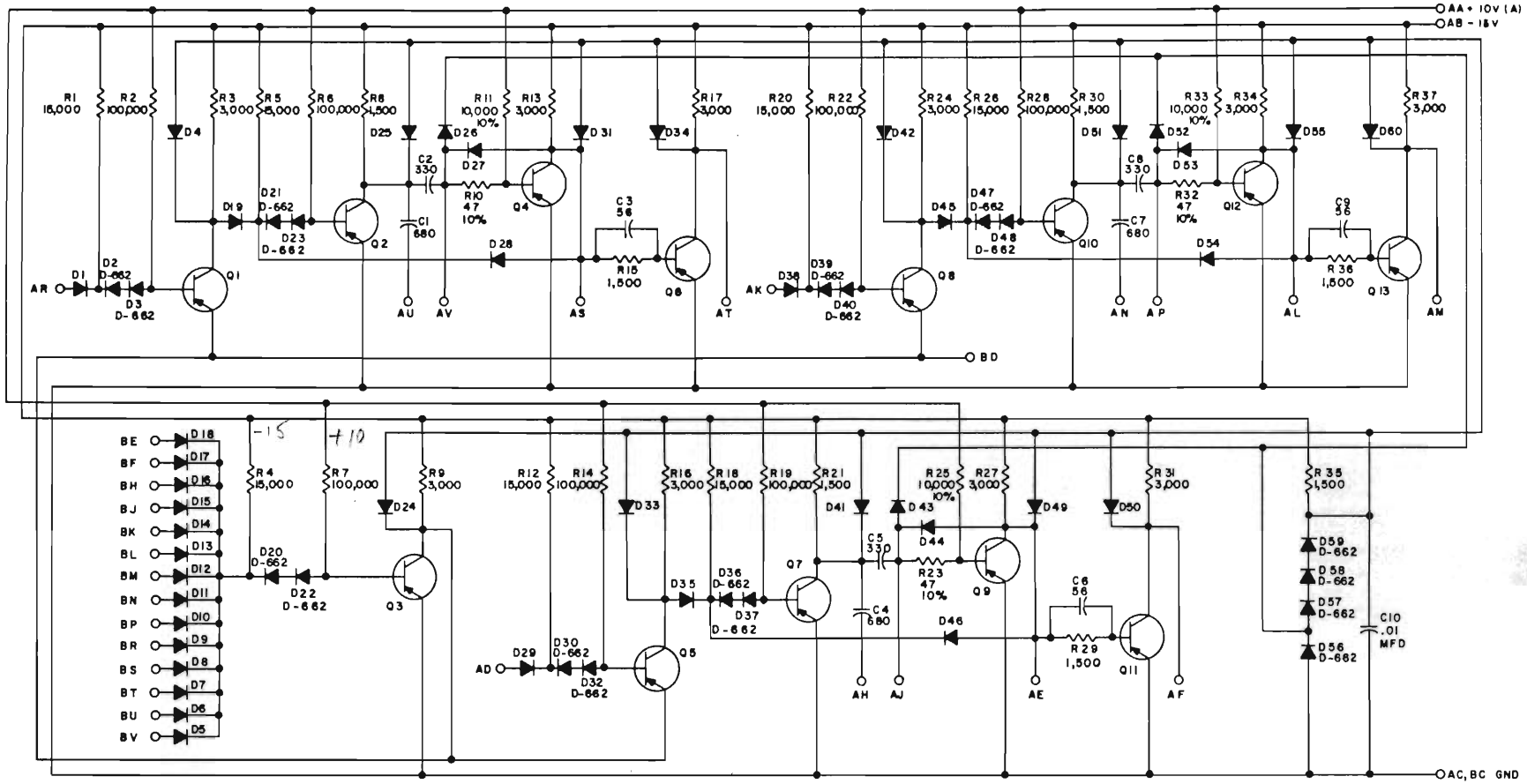


Teletype Connector W070-2



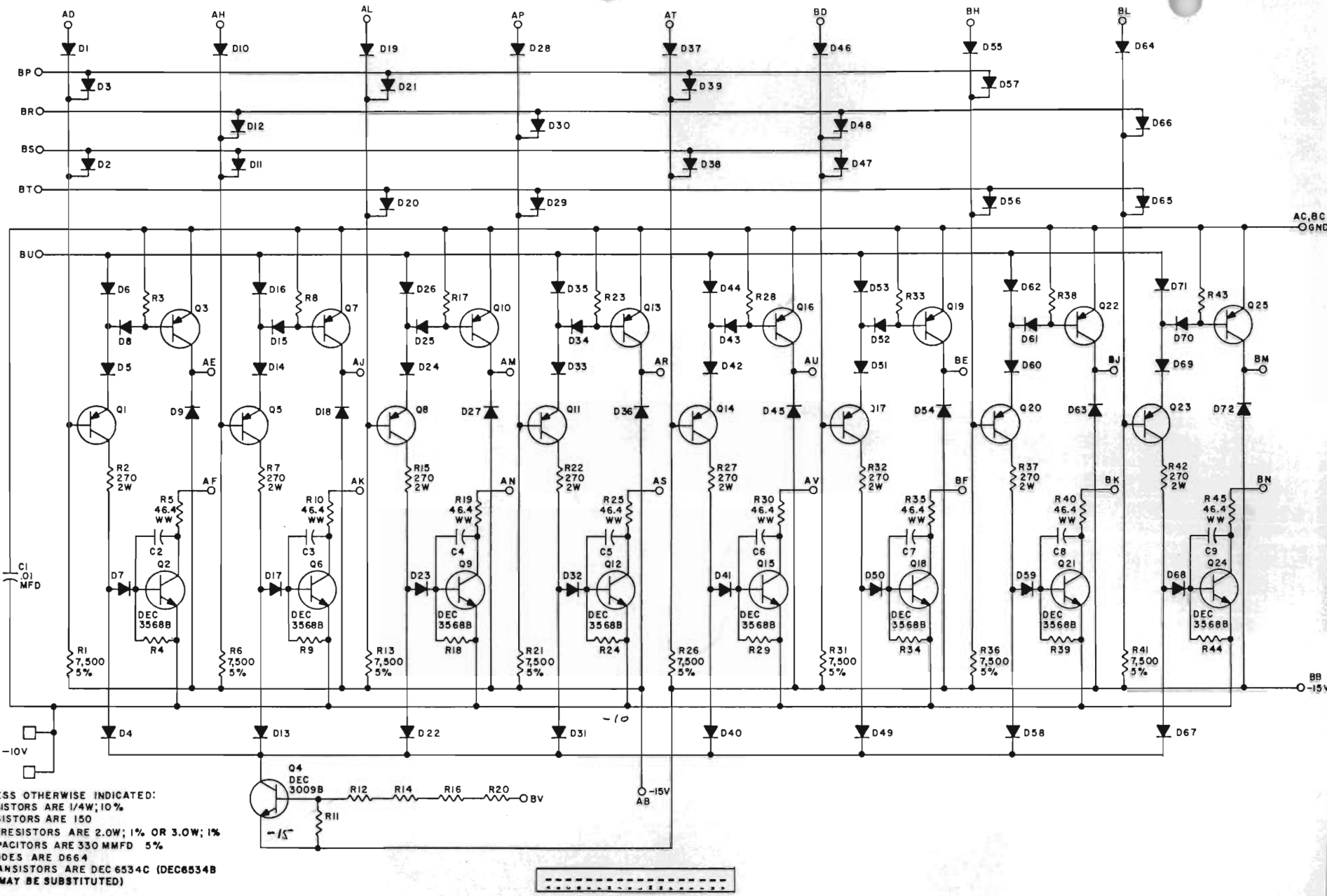
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
TRANSISTORS ARE DEC 2219A
DIODES ARE D664
CAPACITORS ARE 6.8 MFD
35V TANTALUM
TABS ARE AMP 250 SERIES
FASTON TYPE 60145-2
R1 IS A #275P

Power Monitor W506-0-1-A

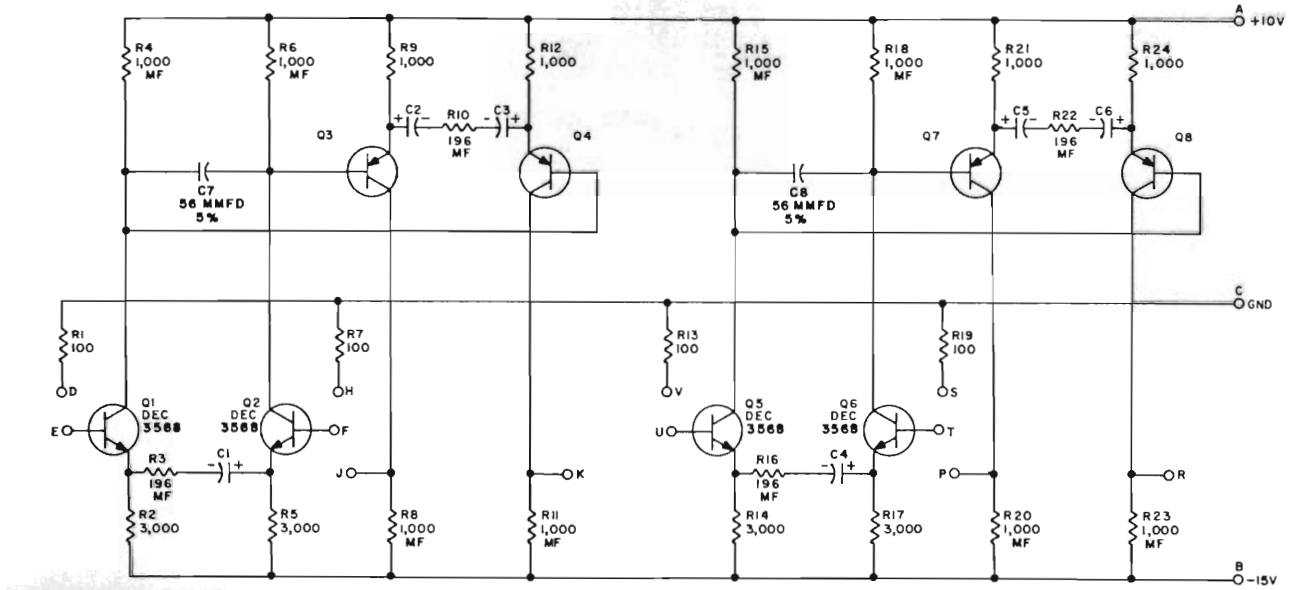


UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4 W, 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

Device Selector W103-3

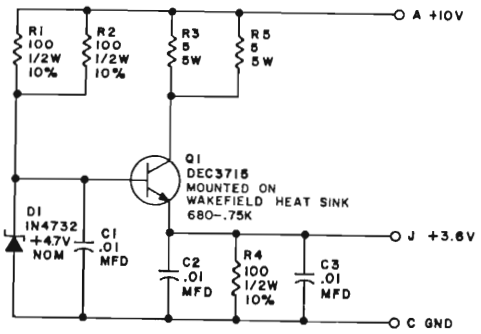


Decoding Driver W108-0-1-A



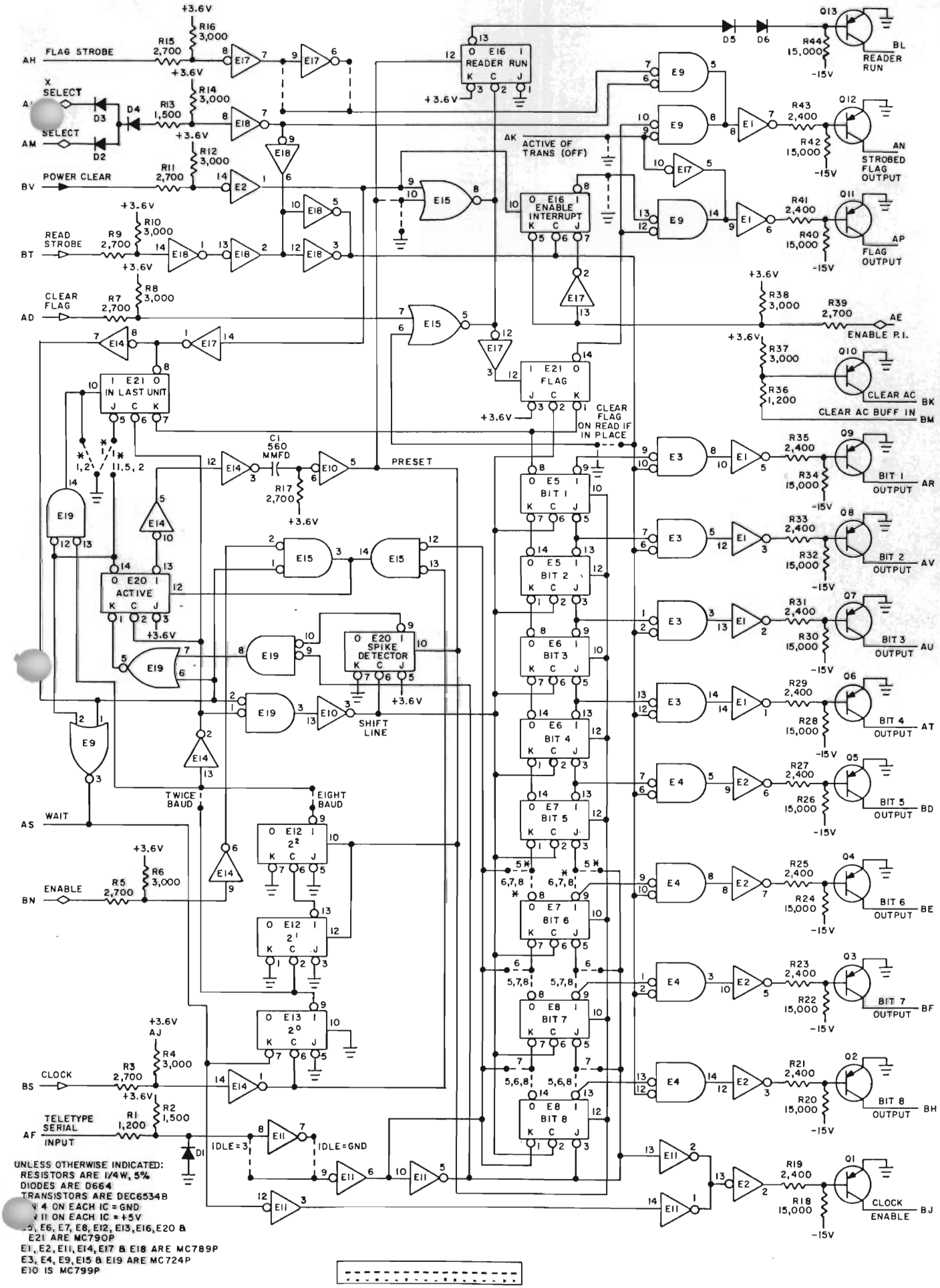
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
MF RESISTORS ARE 1/8W; 1% METAL FILM TO
CAPACITORS ARE 3.9 MFD 10% 10V
TRANSISTORS ARE DEC6534C (DEC6534B MAY BE SUBSTITUTED)

Difference Amplifier W532-0-1-A

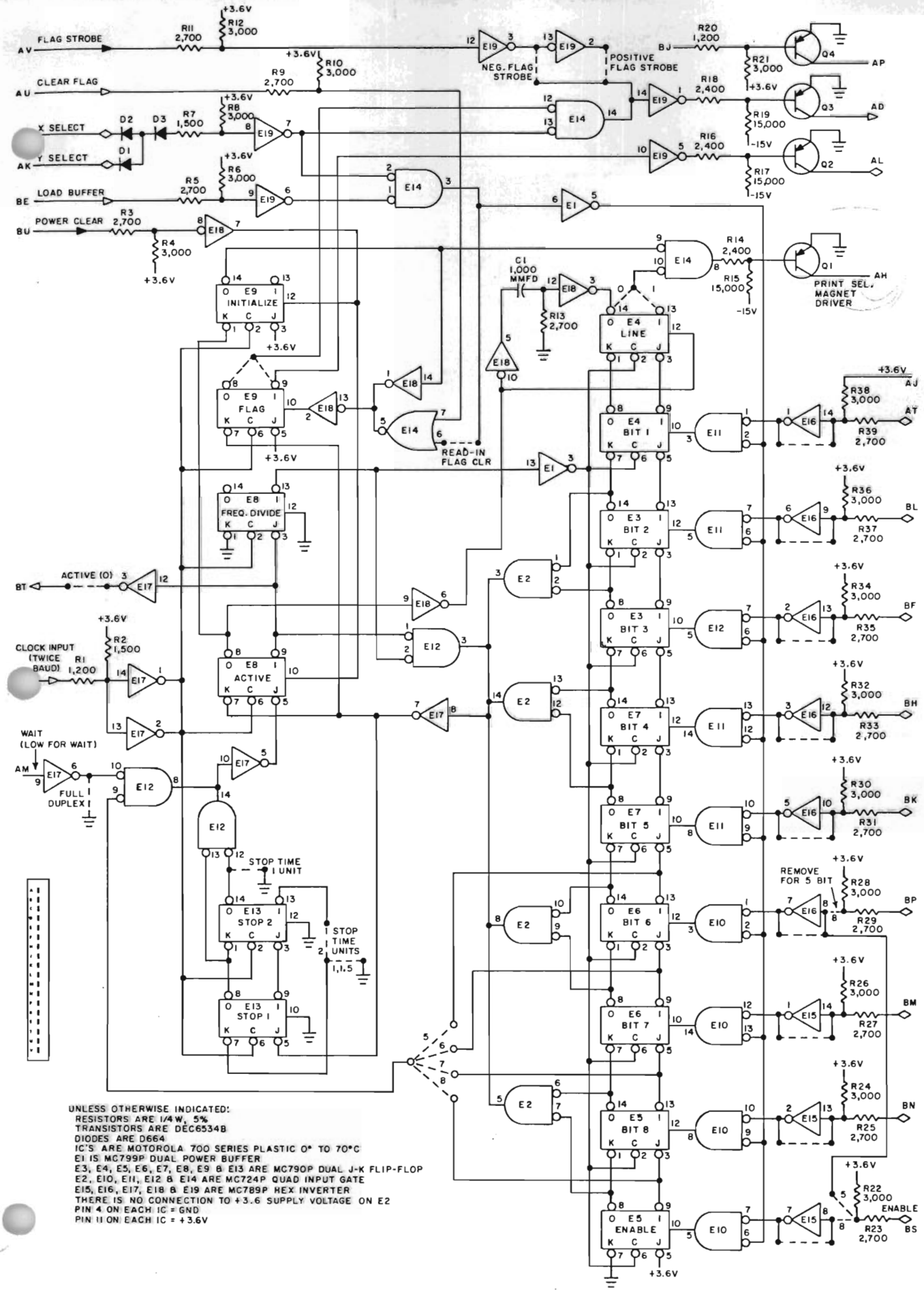


UNLESS OTHERWISE INDICATED:
R3 & R5 ARE WARD LEONARD 5XM5

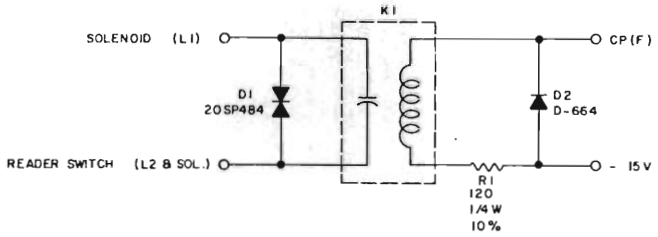
+3.6V Power Supply W705-0-1



Teletype Receiver W706-0-1-C

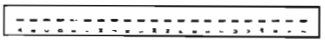


Teletype Transmitter W707-0-1

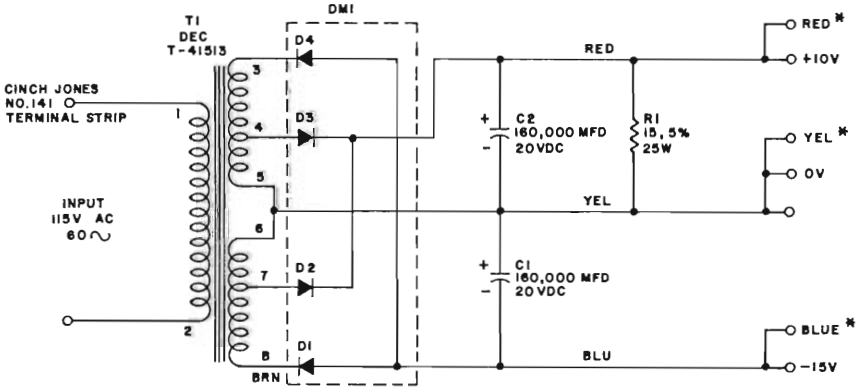


NOTE

K1 - WHEELOCK RELAY 3002-101-12VDC
WITH NO OUTER SHIELD



Teletype Reader Control 4915



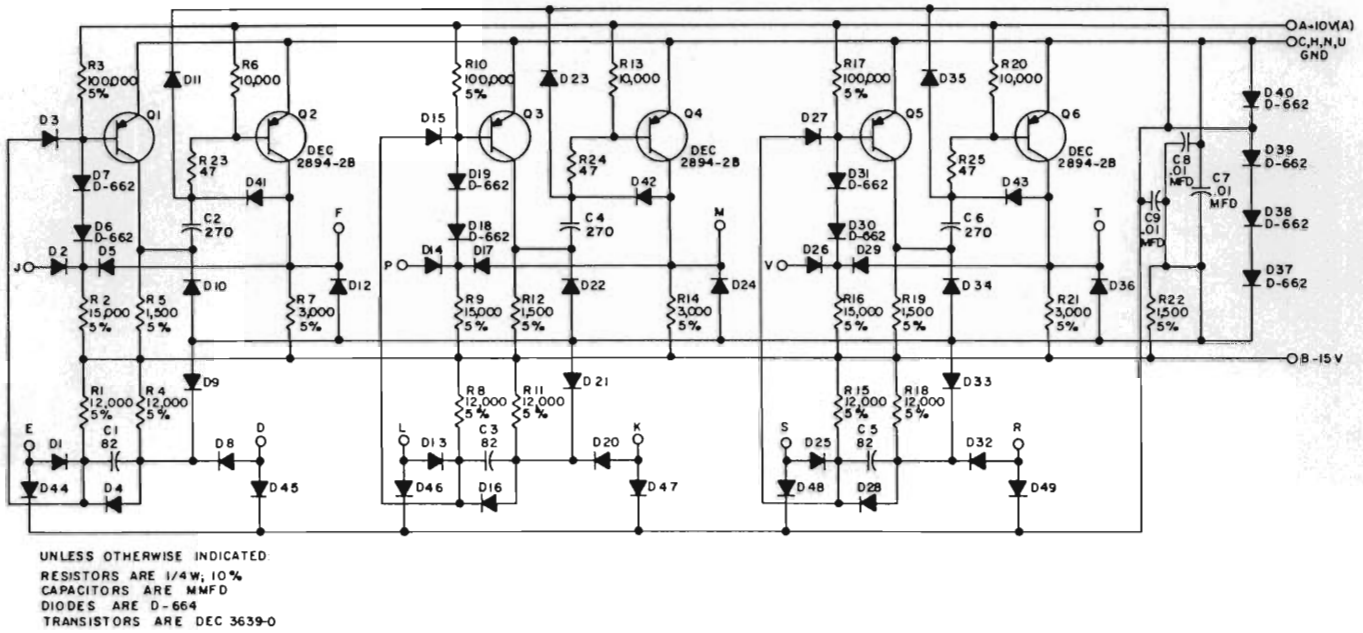
NOTE:
IN ORDER TO KEEP OUTPUT VOLTAGE WITHIN
THE FOLLOWING LIMITS:
+10V: +9.5 TO +11V
-15V: -14.5 TO -16V
THE LOADING SHOULD BE WITHIN THE FOLLOWING LIMITS:

BOTH SIDES LOADED	+10V 0 TO 7.0 AMPS -15V 1.0 TO 8.0 AMPS
ONE SIDE LOADED	+10V 0 TO 7.5 AMPS -15V 1.0 TO 8.5 AMPS

SUM OF THE OUTPUT CURRENTS ARE LIMITED BY
THE EQUATION: $51_{10} + 61_{15} \leq 53$

* HEYMAN MFG. CO. TAB TERMINALS

Power Supply 728



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639-0

Pulse Amplifier S603

APPENDIX B
GLOSSARY

It is not intended that use of this glossary be substituted for reading Chapter 3 or for using the flow charts when following any sequence of events in the logic drawings. The list includes all individual signal names, and for each gives its meaning and the number of the drawing on which it originates. Where no drawing is listed, the item is either a teletype signal (all of which originate on D-BS-PT08-A-1) or is a general abbreviation. No composite signal names are included because these are always made up of standard terms; and no generating conditions are given for logical functions as these are listed in the flow charts. An asterisk indicates that the signal is a pulse.

*A	11	Bit time pulses A00-A13
AC	20	Accumulator
*ACSH	20	AC shift
AI	13	Autoindex flip-flop
AND	16	Logical AND
*AST	15	Auto restart
B		Buffered
BAC	20	Buffered AC
BMB	9	Buffered MB
BT	11	Bit time
C	14	Carry output of adder
CA	14	Carry flip-flop
*CAC	20,17	Clear AC
CFF	15	Clock flip-flop
*CL	10	Clear link
*CLR AC	5,17	Clear AC from I/O channel
*CLK	11	Clock (processor)
CLL	16	Clear link
CLR		Clear
CMA	16	Complement AC
*CMB	9	Clear MB
CML	16	Complement link
CONS	15	Continue key
*CP	15	Continue pulse
DC	15	Deposit (word time)

DCA	16	Deposit and clear
DEPS	15	Deposit key
*DP	15	Deposit pulse
*DPA	15	Deposit pulse delayed
*EP	15	Examine pulse
*EPA	15	Examine pulse delayed
EX	15	Examine (word time)
EXS	15	Examine key
FR	17	Inhibit interrupt during memory field change**
IAC	16	Increment AC
IC	5	Input collector (from bus)
INCPC	13	Increment PC
INCR	13	Increment
INH	18,22	Inhibit level, memory control to core logic
INS	17	Interrupt synchronizer
INT	5,17	Interrupt from I/O channel
IO	17	In-out
I/O	17	In-out
*I/O CLEAR	17	Clear in-out equipment (to bus)
IOF	17	Interrupt off
ION	17	Interrupt on
*IOP	17	In-out pulse (to bus)
*IOSKP	17	In-out skip (from bus)
*IOSKS	17	In-out SKP set
IOT	16	In-out transfer
IR	16	Instruction register
*IR CLR	16	IR clear
ISZ	16	Increment and skip on zero
JMP	16	Jump
JMS	16	Jump to subroutine
L	20	Link
LAS	15	Load address key
LD	15	Load (word time)

**Used only with OMD8S

*LP	15	Load pulse
*LPA	15	Load pulse delayed
LPC	17	Low power condition
*LSH	10	Link shift
MA	12	Memory address
MAB	12	MA buffered
*MASH	12	MA shift
MB	9	Memory
*MBSH	9	MB shift
*MEM	4,23	Memory output pulses to MB and PB
MEMGO	18,22	Level that turns on memory clock
*MPC	17	Memory power clear
*MR	13	Memory request
OP	16	Operate
OP1	16	Operate group 1
OP2	16	Operate group 2
PIR	16	Operate
PB	9	Parity bit
PC	19	Program counter
*PCP	15	Power clear pulse
*PCSH	19	PC shift
PE	9	Parity error
PESEL	17	PE select (IOT)
*PE SET	9	Pulse that sets PE if PT and PB differ
PG	9	Parity generator
PGZ	12	Page zero
PIR	17	Program interrupt request flip-flop
PISEL	17	Program interrupt select (IOT)
*PPC	17	Processor power clear
PSM		Teletype print selector magnet
PT	9	Parity test
RCLE		Teletype receiver clock enable
*RCLO		Teletype receiver clock
RD		Read
READ	18,22	Read level, memory control to core logic

RIAC	20	Readin AC
RIMA	12	Readin MA
RIMB	9	Readin MB
RIPC	19	Readin PC
ROTL	16	Rotate left
ROTR	16	Rotate right
RRE		Teletype reader run
*RT	11	Reset timer
RUN	15	RUN flip-flop
*SAC	10,15	Set AC (from SR)
SAI	13	Sense autoindex
SIK	15	Single instruction switch
SKP	10	Skip flip-flop; skip from I/O channel
*SL	10	Set link
*SP	15	Start pulse
*SP	17	Special pulse (for IOP)
SSK	15	Single step switch
STOS	15	Stop key
*STROBE	18,22	Strobe, memory control to core logic
STS	15	Start key
S	14	Sum output of adder
SR	15	Switch register
SX	14	X-input to adder
SY	14	Y-input to adder
T	11	Timer (time ring counter)
TAD	16	(Two's) add
*TCLO		Teletype transmitter clock
*TP	15	Trigger pulse
*TSH	18,22	Time shift (memory clock output)
TSO		Teletype serial output
WR		Write
WRITE	18,22	Write level, memory control to core logic
WT	13	Word time
WTB	13	Word time break
WTD	13	Word time defer

WTE	13	Word time end
WTF	13	Word time fetch
WTI	13	Word time index
WTINCPC	13	Increment PC
WTINCR	13	Increment
*WT MEM C/W	13	Start clear-write cycle (to memory)
*WT MEM R/W	13	Start read-write cycle (to memory)
WTRD	13	Word time needs to read (from memory)
WTS	13	Word time stop (for memory cycle)
WTWR	13	Word time needs to write (in memory)
WTX	13	Word time execute
ZI	14	Zero indicator

2/16/77 [illegible]

ADJ PWR TO -12.0 AT 67°F

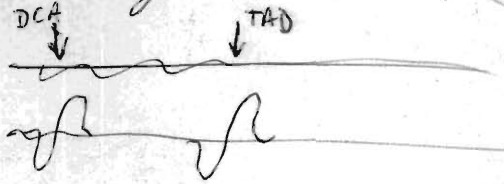
ADJ MEM CYCLE (→ MEMCOL) TO 6.5 μsec.

bit 3 picks

bit 10 drops.

look differentially at sense windings out of G609 (D24)

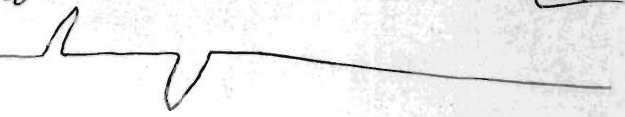
10 mv. scale. bit 11 0 –



1 –

bit 10 0 –

1



THIS INDICATES TAD IS READING THIS BIT BUT NOT RESTORING IT. LOSS ON INPUT TO MB?

program:

0/ 410
1/ 400
400/ 7604
401/ 3400
4021 1400
4031 5401

CAS
DCA I 6
TAD I 6
JMP I 1

SYNC on D39L – WT MEM C/W ch. 18

· bit 3 ⇒ no change on sense lines when bit in switch register toggled. May be losing on inhibit?

Yup No output C345 C340 is OK.

1033 G609 grossly hot power transistor.

BIT 10 – WAS PIECE OF SHIT IN THE CONNECTOR BLOCK. WINNING NOW.

BIT 3 –

~~Exch CD34 ⇔ CD35 W108~~ Exch

Replaced Q11 C34 W108, Exch

W532 6803

C25

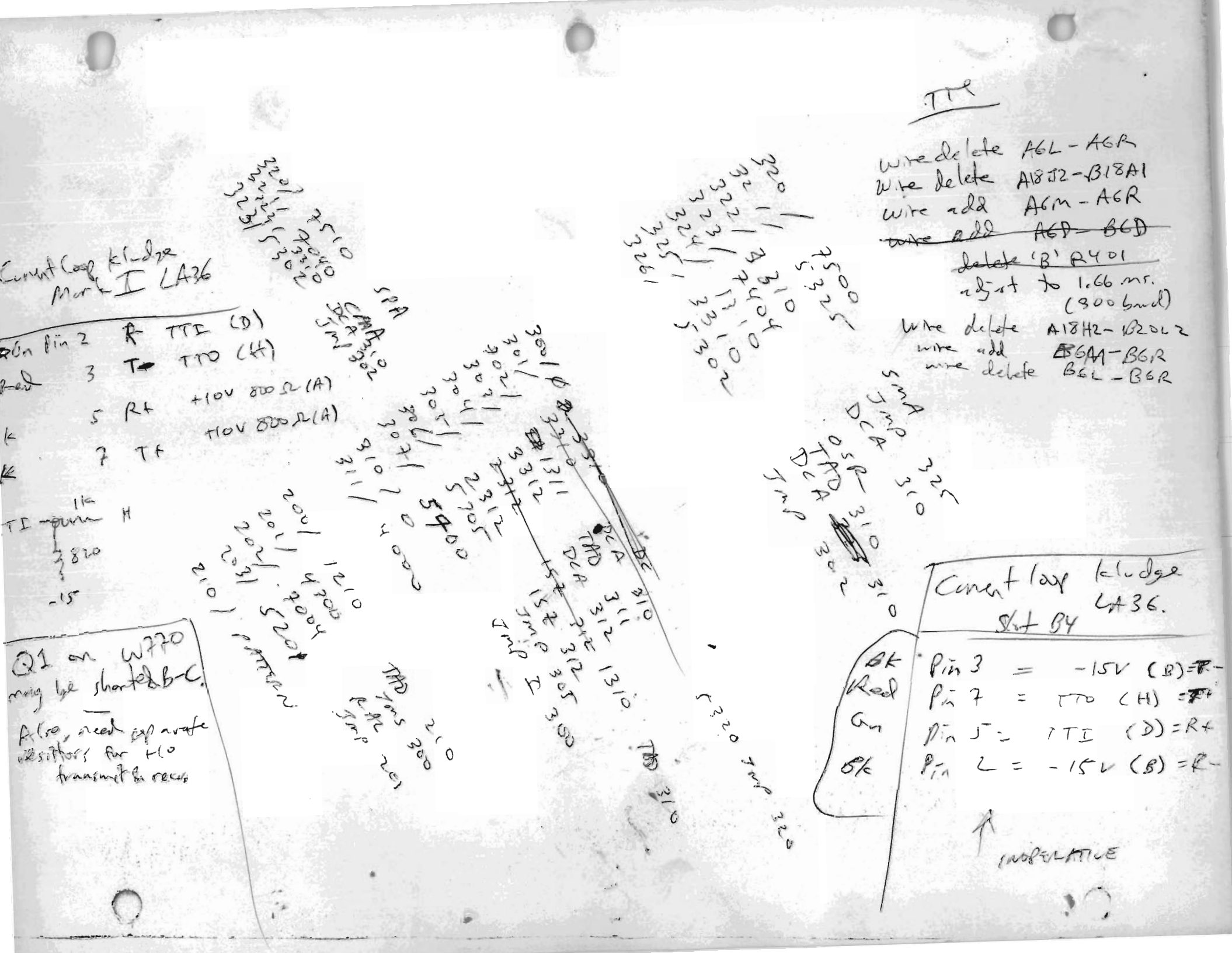
C27 D25

D27

7320
2210
5200
7004
5200

177 1
200 1
201 1
2021
2031

CLA STC
ISZ 210
JMP .-1
RAZ-
JMP 200


TTY
wire delete A6L - A6R
wire delete A18J2 - B18A1
wire add A6M - A6R
~~wire add A6D - B6D~~
~~delete 'B' R401~~
adjust to 1.66 ma. (800 ohms)
wire delete A18H2 - B20L2
wire add B6M - B6R
wire delete B6L - B6R
Current Loop Bridge Mark I LA36
Pin Pin 2 R- TTI (D)
3 T- TTO (H)
5 R+ +10V 800Ω (A)
7 T+ +10V 800Ω (A)
TTI
1K
820
-15
Q1 on W770 may be shorted b-c.
Also, need separate resistors for +10 transmit & recv.
Current loop bridge LA36.
Slot B4
Pin 3 = -15V (B) = R-
Pin 7 = TTO (H) = T+
Pin 5 = TTI (D) = R+
Pin 2 = -15V (B) = R-
BK
Red
Grn
BK
INCREMENTAL