LGP-20

Operators and Maintenance
Manual

Comdyna, Inc.

LGP-20

Operators & Maintenance Manual

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1. OPERATING PROCEDURES

1.0 CONNECTION OF EXTERNAL READOUT INSTRUMENTS

The LGP-20 offers a choice of slow and fast time scales. Slow time outputs are normally recorded with an XY plotter or strip chart recorder; fast time outputs are normally displayed by an oscilloscope.

A time base is provided and should be used wherever possible as the X input to an XY plotter or XY oscilloscope. Use of the internal time base offers two advantages. 1. The time base is calibrated to match the integrator time scales. 2. It sweeps across a fixed range of co-ordinates regardless of the time period being plotter or displayed.

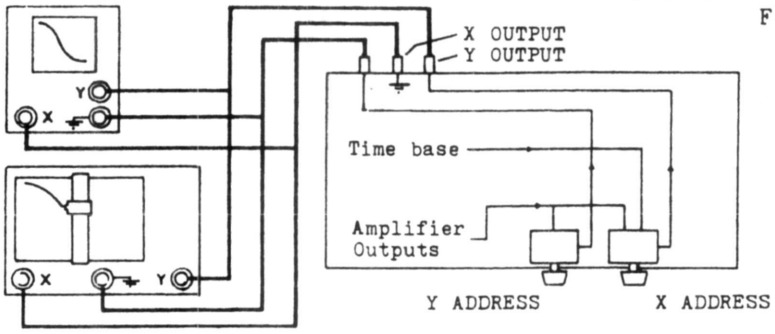


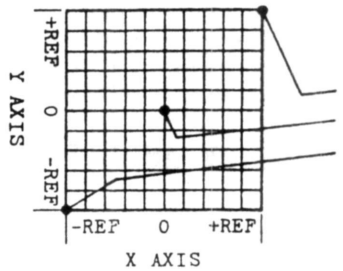
Figure 1-1

Rear binding post terminals offer convenient connections to the X and Y inputs of the plotter and/or oscilloscope. The three connections are shown in Figure 1-1 and listed below.

1. GND...signal ground.
2. Y OUTPUT...selection of the Y ADDRESS switch, to be connected as the plotter and/or oscilloscope vertical input.
3. X OUTPUT...selection of the X ADDRESS switch, to be connected as the horizontal input.

1.1 CALIBRATION OF READOUT INSTRUMENTS

The range and zero position of a plotter or oscilloscope should be selected and positioned so that their full scale horizontal and vertical axes span the LGP-20 minus and plus ten volts reference.



Positive full scale co-ordinate
Center position.
Negative full scale co-ordinate,

The following are procedures for input scaling adjustments:

1. Place the system into the IC mode. (para 1.7.1)
2. Position both the Y ADDRESS and X ADDRESS switches to GND.
3. Adjust the plotter or oscilloscope X and Y zero controls until plotter's pen or oscilloscope's dot is the the graph or display center.
5. Position the Y ADDRESS and X ADDRESS switches to -REF.
6. Adjust the plotter or oscilloscope X and Y gain controls until the pen or dot is the pen or dot negative full scale deflection.
7. Position the Y ADDRESS and X ADDRESS switches to +REF.

8. Check the pen or dot. It should be the positive full scale deflection.
9. Repeat the procedures if necessary.

The readout instruments will either plot or display an amplifier output as a function of time or of another amplifier output, as selected by Y and X ADDRESS switch positions (para 1.5.) Regarding time functions, zero time begins at the negative full scale deflection and sweeps to positive full scale, where the positive full scale deflection equals the compute time period (para. 1.3.)

If the oscilloscope internal time base is used for the repetitive operation display, the fast time scale ratio of 400:1 must be considered: one computer time second equals 2.5 milliseconds real time.

1.2 SETTING COEFFICIENT POTENTIOMETERS

Coefficients are set in IC mode (para 2.3) where a setting is displayed by the digital voltmeter and a selected potentiometer is adjusted until the desired setting is observed. Setting procedures are:

1. Place the system into the IC mode. (para 1.7.1)
2. Complete all patching so that settings are made under their operating loads.
3. Position the DVM SELECTOR switch to POT.
4. Depress the pot set button adjacent to the potentiometer to be set and adjust the potentiometer knob until the desired setting is displayed.

1.2.1 Effects of Amplifier Overrange

An amplifier overrange will alter the setting of any pot patched to the overranged amplifier input. If the overload alarm appears when a pot set button is depressed, remove the overrange condition by patching overranged amplifier outputs directly to their summing junctions. Be sure to remove these patch cords prior to running the program.

1.3 SETTING THE COMPUTE TIME PERIOD

The Compute Time Period is the time taken by the internal time base to sweep from minus to plus reference, the full scale X axis co-ordinate of plotted or displayed time response curves. It is adjustable from 10 to approximately 100 computer time seconds by the COMPUTE TIME control. Setting procedures are:

1. Place the system into the IC mode. (para 1.7.1)
2. Position the Y ADDRESS to TIME, the DVM SELECTOR switch to AMP.
3. Depress the pot set button adjacent to the COMPUTE TIME potentiometer and adjust the knob until the desired compute time period (displayed value times one hundred) is displayed.

1.4 DIGITAL VOLTMETER MEASUREMENTS OF AMPLIFIER OUTPUTS

To measure static values of amplifier outputs:

1. Position the DVM SELECTOR to the AMP position.
2. Position the Y ADDRESS switch to the number of the amplifier output to be measured.
3. Read the display.

1.5 SETTING INITIAL CONDITIONS

Each GP-10 integrator has an initial condition potentiometer and set up toggle switch. To set an initial condition:

1. Measure with the DVM the integrator output. (para 1.4)
2. Set the adjacent toggle switch to plus or minus.
3. Adjust the potentiometer knob until the desired value is displayed.

1.6 MEASUREMENT OF THE SUM OF INTEGRATOR INPUTS

In accordance with program static check requirements, to measure the sum of integrator inputs:

1. Place the system into the IC mode. (para 1.7.1)
2. Patch the SJ jack of the integrator input to be measured to the SJ jack of an unused amplifier patched as a summer-inverter. The summer may require either a 1 or .1 feedback resistor depending upon the output resulting from the borrowed network.
3. Place the system into the HD mode. (para 1.7.2)
4. Measure the amplifier output. (para 1.4)

1.7 MODE CONTROL

The following system integrator modes are controlled by depressing one of the four MODE CONTROL push buttons.

1.7.1 IC...Initial Condition Mode, initial condition values are applied to integrators. (para 1.5)

1.7.2 HD...Hold Mode, integrators hold values at the instant the hold mode logic is applied.

1.7.3 OP...Operate Mode, integrators are placed into a slow time run condition. (1:1 time scaling)

1.7.4 RO...Repetitive Operation Mode, integrators are placed into a high speed condition (400:1 time scaling) and alternately placed into the initial condition and operate modes so that repeated solutions are superimposed as a solid curves on an an oscilloscope display.

*Note: The OP (mode control) Bus originates at the MICROHYBRID I patch panel. Logic generated by the above operations is first directed to the OP and OP blue input MODE CTL jacks. To operate the system from these panel operation it is necessary to patch the blue and orange OP to OP jacks and HD to HD jacks together.

1.8 PROBLEM SOLUTION

The typical analysis of an analog computer simulation is to evaluate the response curves of dependent variables (ampliier outputs) as functions of the independent variable (time.)

To produce time response curves:

1. Y Axis... Position the Y ADDRESS to amplifier output that is to be the ordinate.
2. X Axis... Position the X ADDRESS switch to TIME, the abscissa. (The wiper of the Y ADDRESS switch is connected to the rear terminal Y OUTPUT.)

Oscilloscope Display:

3. Place the system into the repetitive operation mode. (para 1.7.4) The entire response curve is displayed.

XY Recorders:

3. Place the system into the initial condition mode. (para 1.7.1) All integrators are placed into an initial condition mode.

4. Place the system into the operate mode. (para 1.7.3) All integrators are simultaneously placed into a run state and a plot of the response curve is drawn.

Evaluation of Time Response Curves Based on Physical Units

Y Axis...Where zero is the center co-ordinate, the full scale co-ordinates are equated to physical units by setting them equal to the amplifier output's scale factor. (The full scale estimated amplitude

assigned to derive a program's scaled equations. An output in physical units equals the amplifier's normalized output value voltage output times the scale factor. (The normalized output assumes 10 volts reference to be unity and all outputs a ratio of the 10 volt maximum.)

X Axis...The full scale X axis co-ordinate is the compute time period in computer time units divided by the program's time scale factor.

Changing the Compute Time Period

If it is determined that the compute time period is either too long or short for convenient display or recording, the COMPUTE TIME control may be adjusted and a new compute time period established. A new compute time period does not affect the response, only the time period of the response. If a convenient readout is not obtainable with the range of compute time period selections, a new program time scale factor must be selected.

To produce dependent variables vs. dependent variable curves:

Plotting or displaying a variable vs. an other variable requires only that the X ADDRESS switch be positioned to the desired amplifier number. In such cases, zero shall be the center co-ordinate; the oscilloscope or plotter plus and minus full scale co-ordinate, like the Y axis scaling, shall be set equal to the amplifier output's amplitude scale factor.

1.9 MICROHYBRID I

1.9.1 COMPARATOR BIAS ADJUSTMENTS

Each of the four COMPARATOR bias adjustments (knobs k1 thru k4) produces a voltage level that is summed with a patched input, producing when positive a comparator output of a logic 1, negative a logic 0. Bias levels are adjusted as follows through a range of -10 to +10 volts.

1. Apply a constant voltage equal to the desired bias level as the patch panel comparator input.
2. Adjust the COMPARATOR bias knob until a comparator state change is observed. To reach the transient position:

   If the output is a logic 0, turn the knob counterclockwise.
   If the output is a logic 1, turn the knob clockwise.

1.9.2 LED INDICATORS

LED's are lit to indicate a logic 1 state.

1.9.3 DIVIDE BY "N" COUNTER PRESET

Thumbwheel switches preset the two, two-decade downcounters. The left hand thumbwheels preset the L COUNTER; the right hand presets the R COUNTER. (While counting the output is a logic 0. When the counter register is zero, the output becomes a logic 1 and remains a logic 1 until the trailing edge of the next input pulse.)

The L COUNTER is preset when patched input R is a logic 0.
The R COUNTER is preset when the blue input OP MODE CTL jack is a logic 0.

1.9.4 OPERATOR CONTROL SWITCHES

All pushbutton switches are a latched-up logic 1, a logic 0 when depressed.

The toggle switch is either a logic 1 or logic 0 as indicated on panel.

1.a SLAVING TWO OR UNITS TOGETHER

When problem requirements exceed the capacity of one LGP-20, two or more units may be slaved into a single operating system.

1. Designate a unit to be the master; others shall then be slaves to the master.
2. Connect a slave cable to the SLAVE connectors of master and slave units.
3. Patch each unit and the interconnections between units.
4. Depress the OP mode control push button(s) on unit(s) designated as the slave(s.)
5. Run the total system from the master.

1.b OVERRANGE

When any of the GP-10 (upper or lower) operational amplifiers exceed either plus or minus reference, the control panel OVERRANGE light will light. (The actual overrange threshold is normally set to about 1.05. See the 970 Overload Indicator circuit description for adjustment procedures.)

In addition to the control panel OVERRANGE alarm, each of the GP-10 patch panels has an LED alarm located in the lower right hand corner.

To determine the amplifier(s) in an overrange condition, first check in which GP-10 the overrange is occurring, then sequentially step through the Y ADDRESS switch and observe amplifier output values. (para 1.4)

1.c POWER

The AC power switch is located at the rear of the unit under the AC power receptacle. A 'power on' condition is apparent by the appearance of the digital voltmeter display.

2. OPERATOR FUNCTIONS

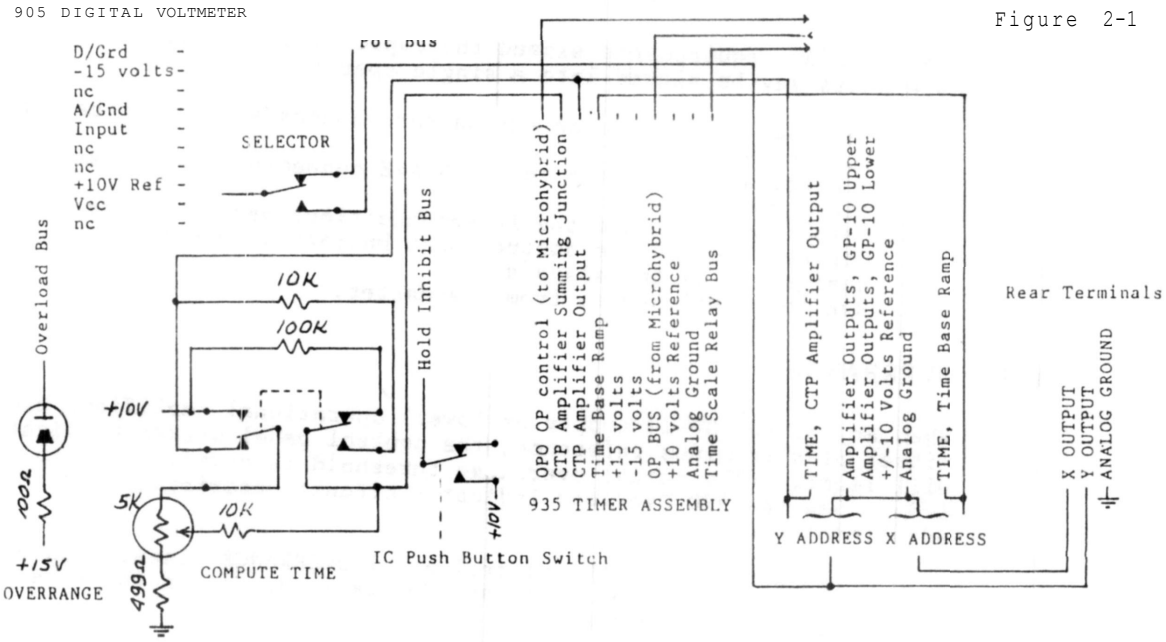


Figure 2-1

Figure 2-1 is a schematic of operator functions. Descriptions of the individual operations are described in the following:

2.1 Y ADDRESS

The Y ADDRESS switch is an 24 position, single pole rotary switch. Contacts 1-8 are connected to lower GP-10 amplifier outputs 1-8, 9-16 are connected to upper GP-10 amplifier outputs 1-8, 17-20 are connected to Microhybrid I amplifiers 1-4, 21 is ground, 22 is -10V, 23 is +10V, 24 is the CTP amplifier output which is the input to the time base integrator output. The wiper is connected to the rear terminal Y OUTPUT and DVM SELECTOR toggle switch, AMP contact.

2.2 X ADDRESS

The X ADDRESS switch is the same as the Y ADDRESS except that the TIME position is the time base ramp. The wiper is connected to the rear terminal X OUTPUT.

2.3 MODE CONTROL

The following system integrator modes are controlled with the four mode control push buttons.

2.3.1 Initial Condition... Depression of the IC push button pulls the OP bus to ground for reset of system integrators.

2.3.2 Hold... Depression of the HD push buttons pulls the OP bus to a hold mode control voltage level (approximately -2 volts) for placement of system integrators into a hold mode condition.

2.3.3 Operate... Depression of the OP push button releases the OP bus to an operate mode control level (-5 to -15 volts) for placement of system integrators into a slow time, operate condition.

2.3.4 Repetitive Operation... Depression of the RO push button places the Time Scale Relay bus into a de-energized state and connects the OP bus to the repetitive operation timing unit mode control.

2.3.5 OP Bus... The system mode control bus, originates at the Microhybrid. Above described operations are changed to TTL logic terminated at the Microhybrid orange OP and HD jacks. For these operations to produce the OP Bus it is necessary to patch the orange to the blue inputs, OP to OP and HD to HD.

2.4 COMPUTE TIME

The COMPUTE TIME control consists of a coefficient potentiometer and a double pole, double throw push button switch that serves to program the CTP amplifier. In a normal operating condition the coefficient adjusts the time base integrator within a range of -10 to -1 volts which produces a compute time period of 10 to 100 computer time seconds.

Depression of the button control rearranges the input and feedback resistor network to produce an output that is an inverse of the released condition.

In the released position, +10 volts is applied through the COMPUTE TIME control (100K ohms) and a series 10K ohm resistor to the CTP amplifier summing junction. A 10K ohm resistor is the feedback. Therefore:

CTP = -10/(CT + 10) x 10 volts.

In the depressed position, +10 volts is applied through a 100K ohm resistor to the CTP summing junction. The COMPUTE TIME control and 10K ohm resistor are the feedback. Therefore:

CTP = -(CT + 10)/100 x 10 volts.

The CTP amplifier output in the depressed position is one tenth the reciprocal of its value in the released position. As the CTP output is the input to the time base integrator, its reciprocal is an indicator of the compute time period.

2.5 DIGITAL VOLTMETER

The digital voltmeter is an +/-10 volts input, 3 1/2 digit resolution, where the decimal point is positioned so that a 10V measurement is displayed as 1.000, in accordance with normalized analog computer scaling methods.

An input to the digital voltmeter is either the Pot Bus (POT) or Y ADDRESS switch wiper (AMP) as determined by the SELECTOR switch position.

2.5.1 Pot Bus Function...When the button adjacent to any system coefficient potentiometer is depressed, the patch panel input to the top of the pot is replaced by +10V reference and the wiper is connected to the Pot Bus.

2.5.2 Hold Inhibit...In the IC mode (para 1.7.1) the Hold Inhibit Bus is switched to +10V to force the hold switches of all integrators to conduct. Without the hold inhibit feature the hold switch shuts off and thereby isolates the input resistor network. As coefficient potentiometers must be set with their programmed resistor loads, it is necessary that the hold switches be on so that the network summing junctions conduct to ground through the shunt FETs. (See 911-3 Quad Amplifier Assembly)

2.6 OVERRANGE ALARM

The panel LED anode is connected to Vcc through a 100 ohm resistor. The cathode is a common to each of the two GP-10 panel LED alarms. Each of these cathodes is pulled to ground when a GP-10 amplifier is in an overrange condition. (See 970-1 Overload Indicator)

2.9 REAR TERMINATIONS

2.9.1 Binding Posts...The three binding posts are identified as Y OUTPUT, ground and X OUTPUT and are terminations for the X and Y address switches wipers and signal ground. (para 2.1 and 2.2.

2.9.2 TRUNKS...Trunks are terminated in three 25 pin type D data connectors, listed below. Facing the rear of the unit, pin 1 is upper row left, pin 14 is lower row left.

	TOP	MIDDLE	BOTTOM
1.	nc	Agnd	nc
2.	nc	MO3	nc
3.	+10V Reference	TR7 (upper GP-10)	nc
4.	-10V Reference	Agnd	nc
5.	Agnd	MO2	I/O4
6.	nc	TR6	I/O2
7.	OP Bus	Agnd	I/O8
8.	nc	TR5	I/O6
9.	TS Relay Bus	TR5	nc
10.	nc	Agnd	nc
11.	Chassis ground	MI4	nc
12.	nc	TR4	nc
13.	nc	nc	Dgnd
14.	nc	TR8	Interrupt
15.	nc	Agnd	RESET
16.	nc	MI3	STOP
17.	nc	TR3	GO
18.	TR1 (lower GP-10)	Agnd	I/O3
19.	TR2	MI2	I/O1
20.	TR3	TR2	I/O7
21.	TR4	Agnd	I/O5
22.	TR5	MI1	nc
23.	TR6	TR1	nc
24.	TR7	Agnd	nc
25.	TR8	MO4	nc

notes:

1. Agnd is analog ground; DGnd is digital ground.

2. TR refers to GP-10 trunks. Trunks from the lower GP-10 are found in the top connector, the upper GP-10 in middle connector.

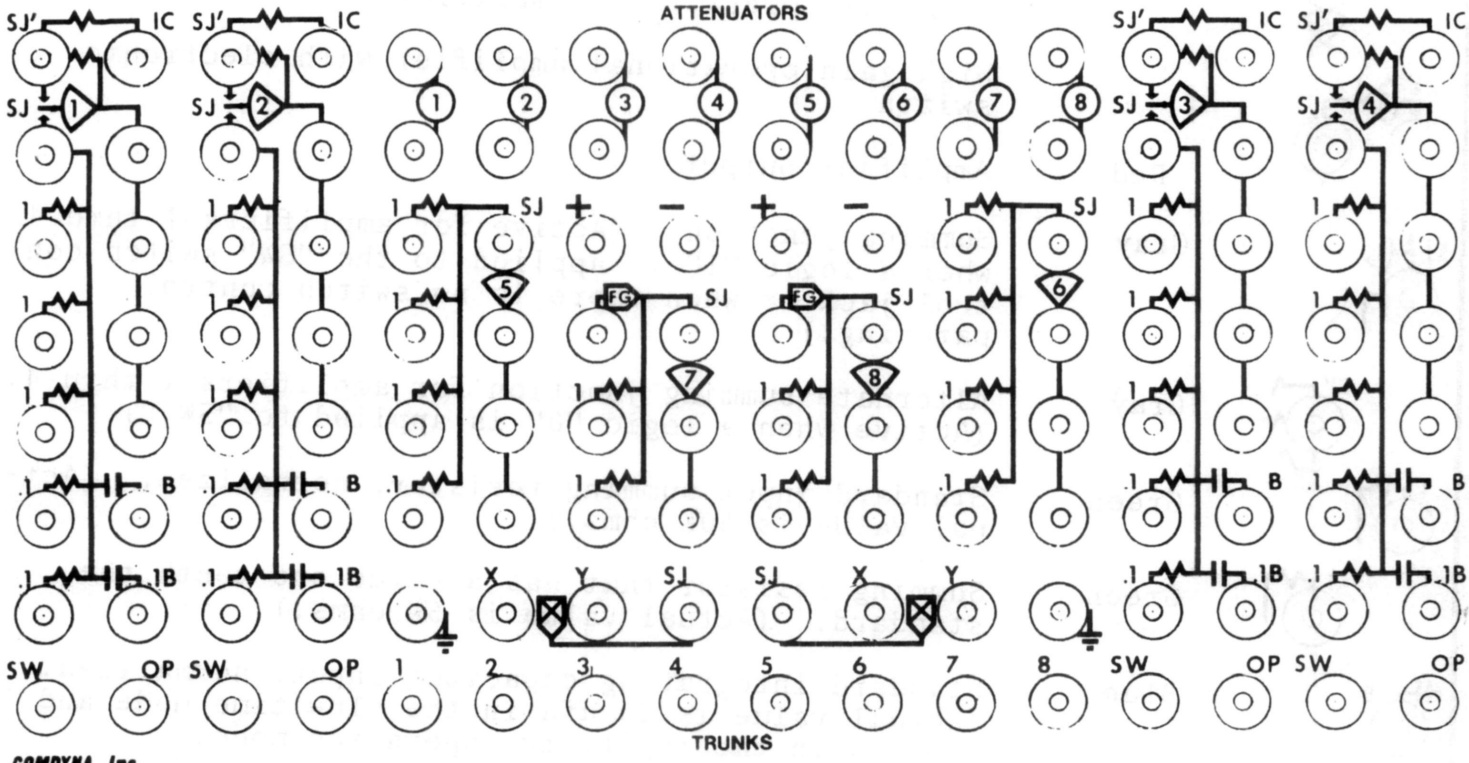
3. MO refers to a Microhybrid MDAC output jack. MI refers to a MICROHYBRID MDAC input jack.

4. I/O refers to the MICROHYBRID I/O BUS jacks.

5. Interrupt is the MICROHYBRID INTERRUPT jack.

6. RESET, STOP and GO are connections to the latch-up push button switches so marked on the MICROHYBRID I panel.

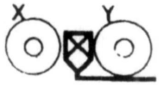
GP-10 ANALOG COMPUTING UNIT



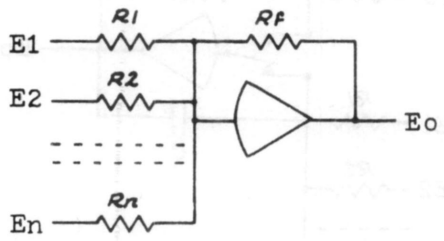
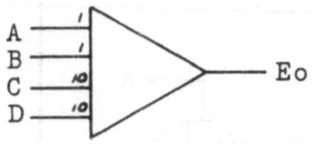
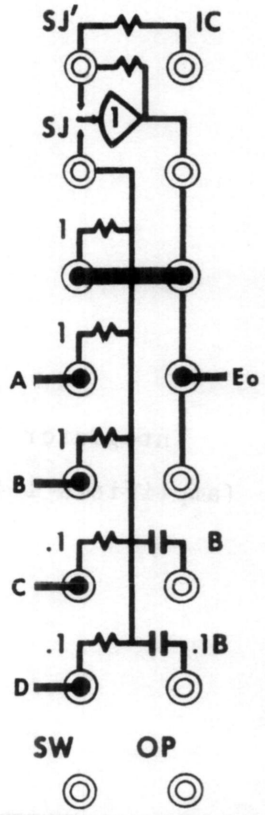
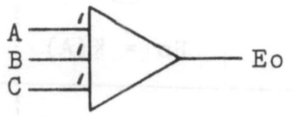
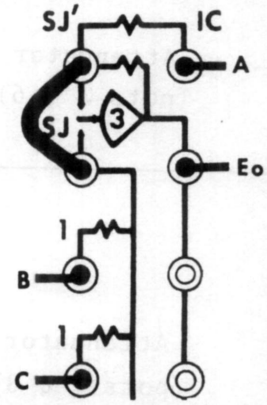
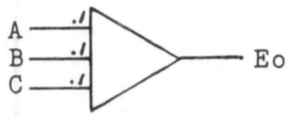
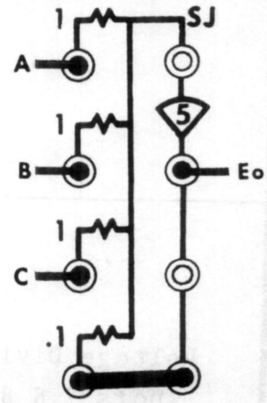
Patch panel graphics represent networks as they are applied in normal analog computer programming. All amplifiers may be used as summers or high gain operational amplifiers; amplifiers 1 thru 4 have electronic switch networks and may be programmed as integrators, track/store amplifiers and single pole, double throw electronic switches. Initial Condition Attenuator wipers are connected to the "IC" inputs for entering manually set constants. Eight Attenuators have their inputs and wipers terminated at the patch panel. Multiplier networks have current outputs; with one amplifier each may be used as a multiplier, divider, squarer or square root extractor. Eight trunk jacks may be used to route external inputs and outputs. The two "FG" trunks that are connected to amplifiers 7 and 8 are reserved for diode function generator inputs.

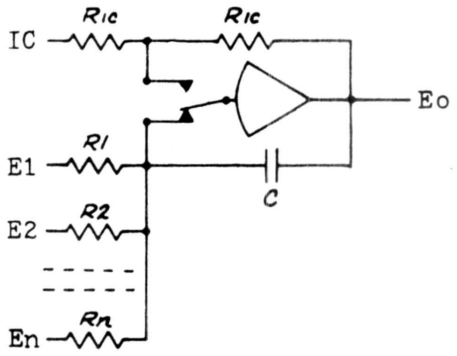
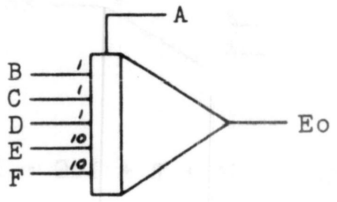
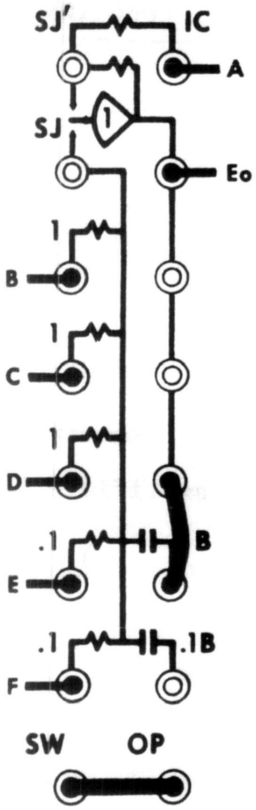
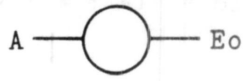
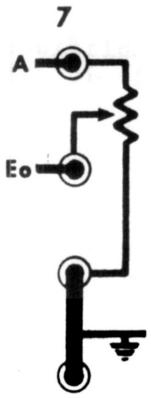
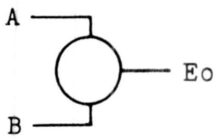
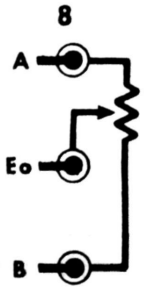
The following is a description of patch panel symbols:

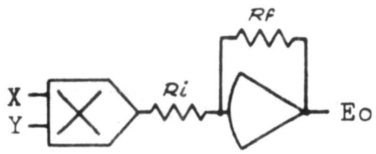
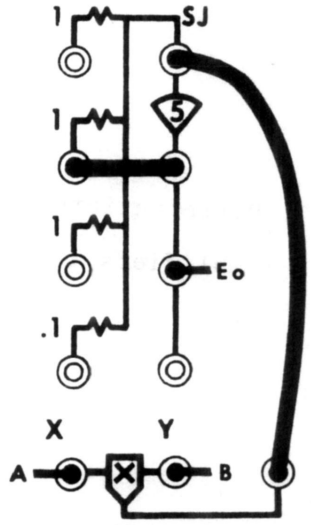
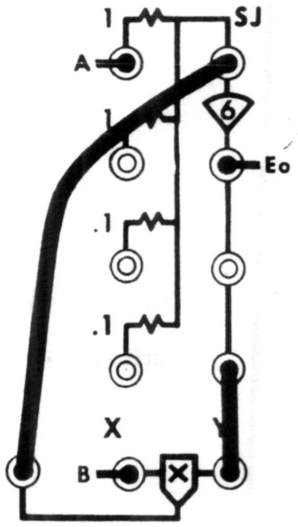
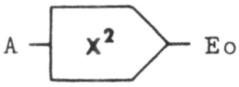
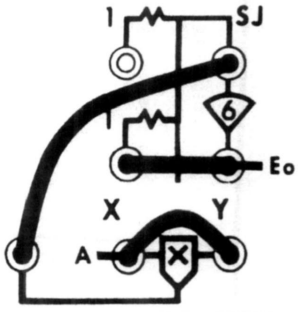
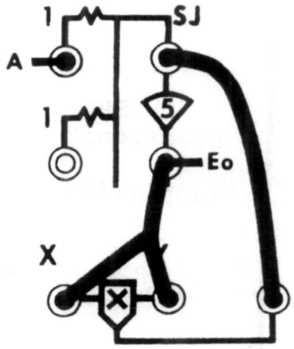
SYMBOL	COLOR CODE	DESCRIPTION
+	Orange	Positive reference, considered unity, 1.000, for formalized programming. (Actual value is 10 volts.)
−	Yellow	Negative reference.
⏚	Black	Analog Signal Ground.
6	Yellow	Manual attenuator input.
	Yellow	Manual attenuator wiper or output.
4 TRUNKS	White	Trunk lines. Routing determined by user.

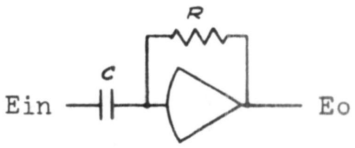
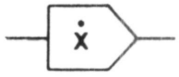
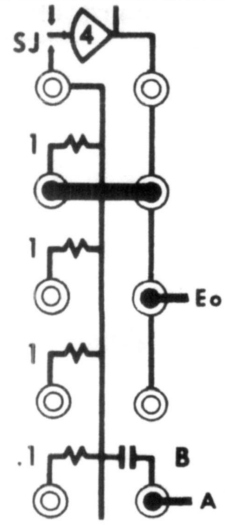
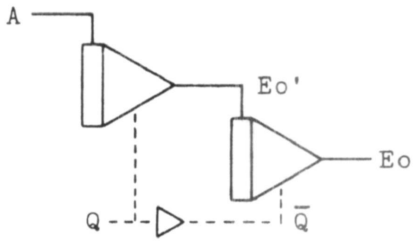
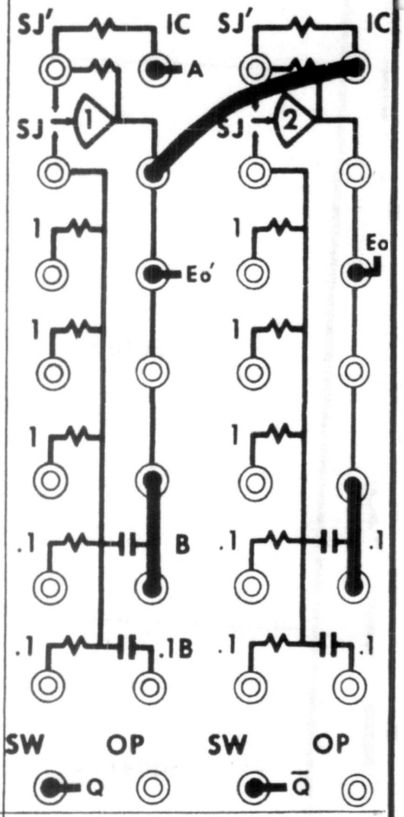
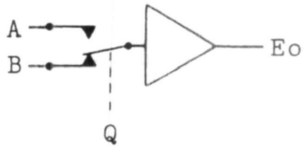
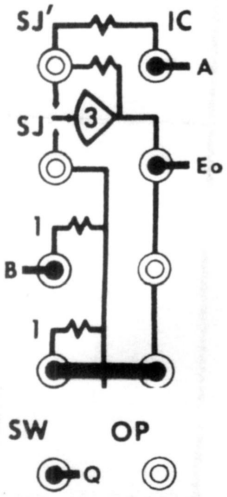
SYMBOL	COLOR CODE	DESCRIPTION
		High gain operational amplifier.
		High gain operational amplifier with electronic switch.
	Red	Amplifier output.
	Gray	Summing junction. (Active for amplifiers 1 thru 4 when a logic "1" is applied to the "SW" switch control jack or when there is no switch control patching.)
	Gray	Alternate summing junction for amplifiers 1 thru 4. (Active when a logic "0" is applied to "SW.")
	Green	Standard input summing resistor, normalized. (Actual value is 50K ohms.)
	Green	Summing resistor that has a value one tenth the standard. (Actual value is 5K ohms.)
	Blue	Standard integrating capacitor input, normalized. (Actual value is 20 ufd in the slow time mode and .05 ufd in the repetitive operation mode.)
	Blue	Integrating capacitor that has a value equal to one tenth the standard. (Actual value is 2 ufd in the slow time mode and .005 ufd in the rep. op. mode.)
	Green	Resistor network. Amplifier becomes an inverter when SJ' is active. When SJ is active, amplifier may be a summer by patching SJ and SJ' together. "IC" jack is the normal integrator initial condition input as it is connected to the associated Initial Condition Attenuator wiper. (Value of resistors is 50K ohms.)
	White	Electronic switch control input. With a logic "0" (ground or positive voltage) the SJ' summing junction is active and SJ shuts off. With a logic "1" (-5 thru -15 volts) SJ is active and SJ' shuts off. With "HD" logic (-2 thru -3 volts) SJ' shuts off, the SJ summing junction is active but the summing resistor network is disconnected.
	White	The system's operate bus; provides integrator mode control logic as selected by the operator.
	Brown	Multiplier network. "X" and "Y" are inputs.
	Gray	Multiplier output, a current that is proportional to the product of inputs "X" and "Y."
	Brown	Trunks allocated as function generator inputs to amplifiers 7 and 8.

PATCH PANEL OPERATIONS

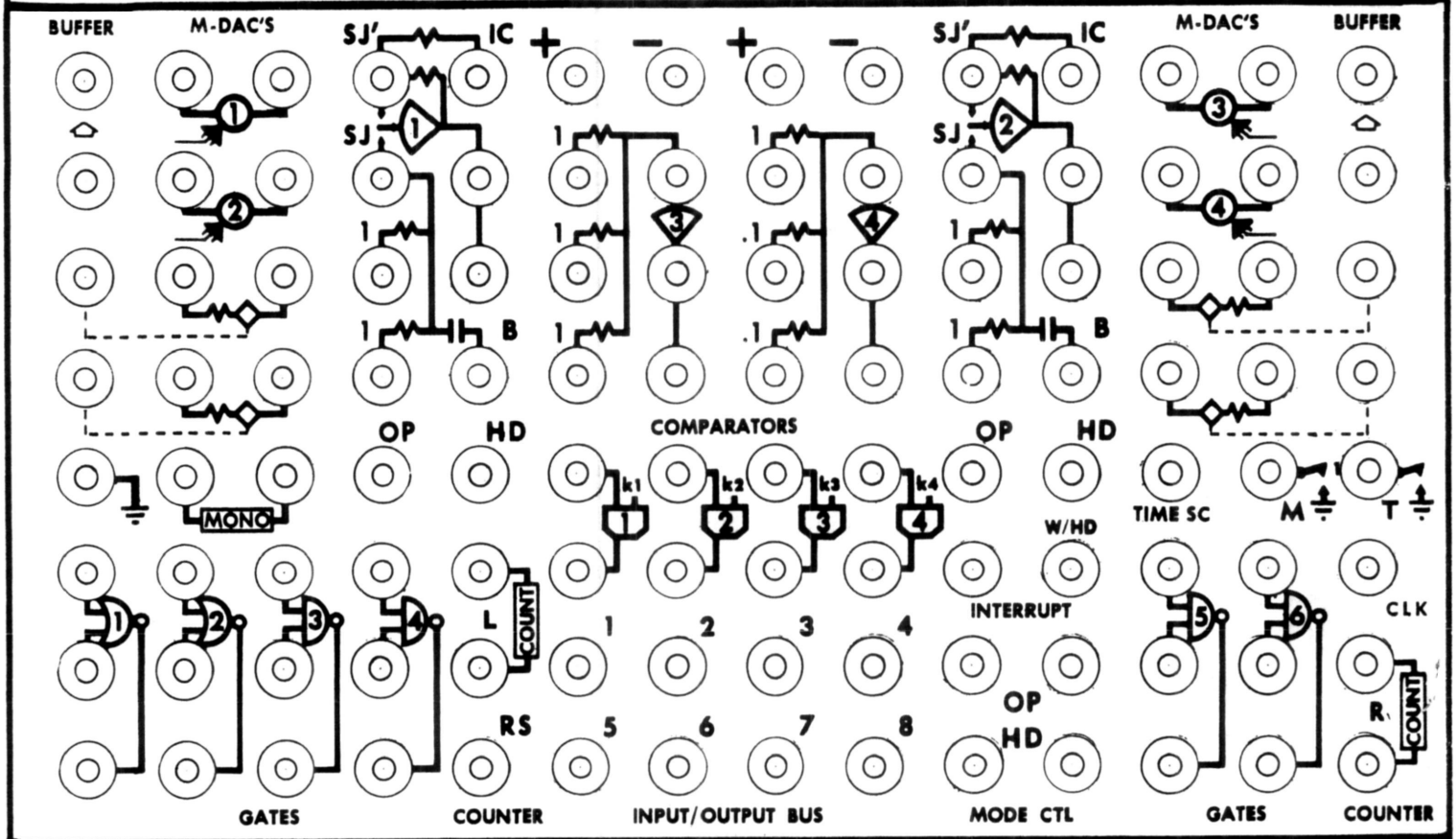
FUNCTION	OPERATION	PATCHING
Summer (amplifiers 1-4)	Fundamental Summer Operation  Eo = -Rf(E1/R1 + E2/R2 ... + En/Rn)  Eo = -(A + B + IOC + 10D) NO PATCHING TO SWITCH CONTROL "SW"	
Summer (amplifiers 1-4 with IC networks)	 Eo = -(A + B + C) NO PATCHING TO SWITCH CONTROL "SW"	
Summer (amplifiers 5 & 6)	 Eo = -(.1A + .1B + .1C)	
Inverter (amplifiers 7 & 8)	Eo = -A	

FUNCTION	OPERATION	PATCHING
Integrator (amplifiers 1-4)	Fundamental Integrator Operation  $Eo = -1/C\int(E1/R1 + E2/R2 \ldots + En/Rn)dt - IC$  $Eo = -\int(B + C + D + 10E + 10F)dt - A$	
Attenuator (pots 1 - 6)	 Eo = K(A)	
Attenuator (pots 7 & 8)	 Eo = K(A)	
Voltage Divider (pots 7 & 8)	 Eo = K(A - B) + B	

FUNCTION	OPERATION	PATCHING
Multiplier	Fundamental Multiplier Operation  Eo = -(X*Y)  Eo = -(A*B)	
Divider	 Eo = -(A/B) A > 0	
Squarer	 Eo = -A²	
Square Root	 Eo = -√A A < 0	

FUNCTION	OPERATION	PATCHING
Differentiator (amplifiers 1-4)	Fundamental Differeniator Operation  Eo = -RC•dEin/dt  Eo = -dA/dt NO SWITCH CONTROL PATCHING	
Track/Store (amplifiers 1-4)	 Eo' = -A when Q is a logic 0 Eo' = -A* when Q is a logic 1 A' is the stored value of A when Q switches from 0 to 1 Eo = A'(n-1) A'(n-1) is the previous value of A'	
SPDT Electronic Switch (amplifiers 1-4)	 Eo = -A when Q is a Logic "0" Eo = -B when Q is a Logic "1"	

MICROHYBRID I PATCH PANEL LAYOUT

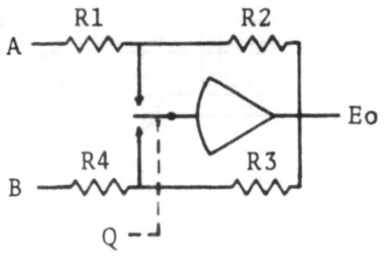
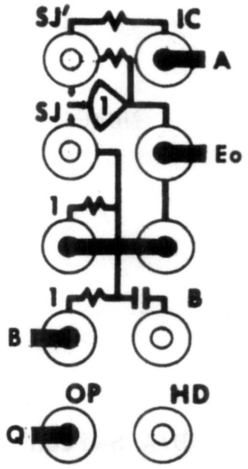
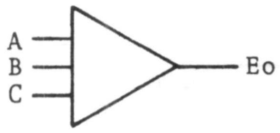
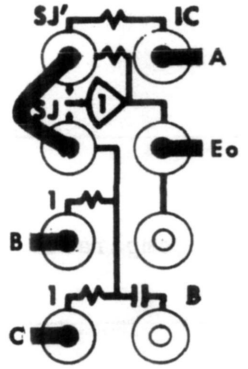
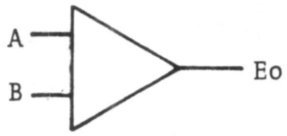
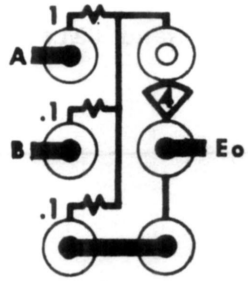
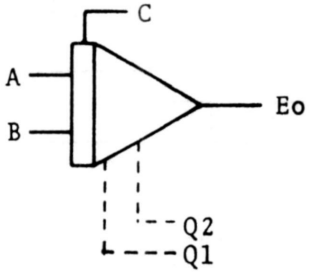
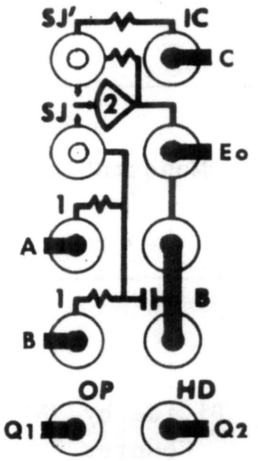


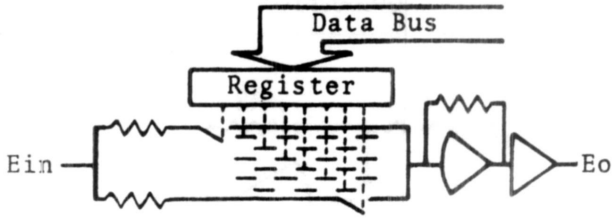
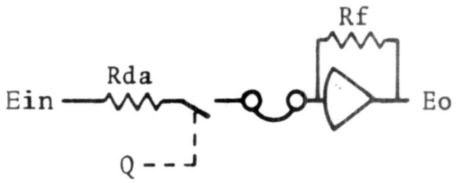
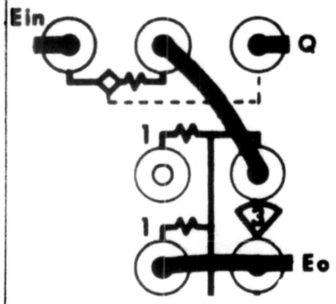
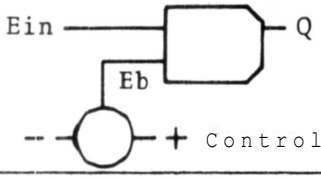
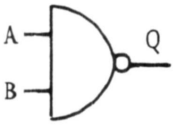
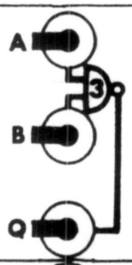
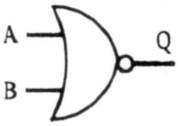
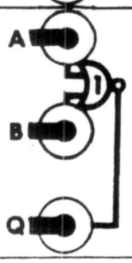
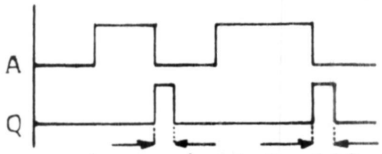
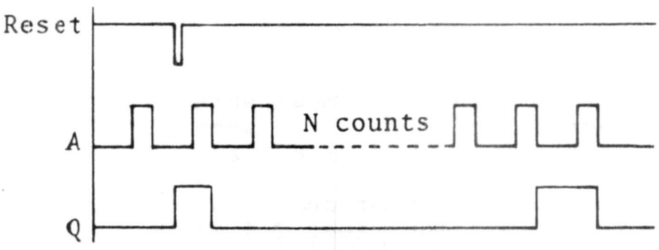
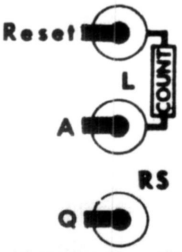
The following are descriptions of Microhybrid patch panel symbols and color codes.

SYMBOL	COLOR CODE	DESCRIPTION
+	Red	Positive reference (+1.000 normalized or +10.00 volts.)
−	Yellow	Negative reference (-1.000 normalized or -10.00 volts.)
2		High gain operational amplifier with electronic switch.
	Red	Amplifier output.
SJ 1	Gray	Amplifier summing junction. (Active for amplifiers 1 & 2 when switch control "OP" is a logic 1 or with no patching.)
SJ'	Gray	Alternate summing junction for amplifiers 1 & 2. (Active when "OP" is a logic 0.
1	Green	Standard input summing resistor, normalized as a unity value to simplify programming. (Actual value is 50 K ohms.)
.1	Green	Summing resistor input that has a value one tenth the standard. (Actual value is 5 K ohms.)
B	Green	Standard integrating capacitor input, normalized so that the 1 resistor and B capacitor combination produces a one second time constant as referred to programming time scales. (Actual value is 20 ufd in the slow time mode and .05 in the high speed mode.)
IC	Green	Resistor input to the SJ' summing junction. Amplifier becomes an inverter when SJ' is active. Normally used for integrator initial conditions. Input and feedback resistors may be used for summer operation by patching SJ' to SJ. (Actual value of input and feedback resistors are 50 K ohms.)

SYMBOL	COLOR CODE	DESCRIPTION
	White	Electronic switch control for the above amplifier. With a logic 0 (ground) the SJ' summing junction is active and SJ shuts off. With a logic 1 (Vcc) SJ is active and SJ' shuts off.
	White	Electronic Hold mode control. When "OP" is a logic 1 and "HD" is a logic 1, the above amplifier, programmed as an integrator, is switched into a hold mode condition.
	White	Buffer output, ground and -15 volts for logic 0 & 1 input.
	Violet	Buffer input.
	Green/Gray	D/A switch input/summing junction connection. (On value is the same as the standard "1" input summing resistor.)
	White	D/A switch control. (On with logic 0; off with logic 1.)
	Green/Red	MDAC input/output.
	Green	Comparator analog input.
	Orange	Comparator logic output. (Positive analog is a logic 1)
	Blue	NAND gate inputs.
	Orange	NAND gate output.
	Blue	NOR gate inputs.
	Orange	NOR gate output.
	Blue	Divide by "N" counter input.
	Orange	Divide by "N" counter output.
	Violet	Presets counter to thumbwheel "N" setting.
	Blue/Orange	Monostable input/output.
	Orange	Analog computer to logic IC/OP mode indicator. (OP is logic 1)
	Blue	Logic control of analog computer IC/OP modes. (Logic 1 for OP)
	Orange	Analog computer to logic HD mode indicator. (HD is logic 1)
	Blue	Logic control of analog computer HD mode. (Logic 1 for HD)
	Violet	High/low transient sets interrupt bit latch.
	Violet	High/low transient sets interrupt bit and analog computer hold mode latch.
	Violet	Analog computer time scale relay control. (Slow time with logic 0; fast time with logic 1)
	Violet	One second pulses referred to the analog computer time scales
	Yellow	Control panel momentary switch termination. (Depressed push button is a logic 0; released button is a logic 1.)
	Yellow	Control panel toggle switch termination.
	Brown	Eight terminations that may be set or read by the digital computer as a data word.

PATCH PANEL OPERATIONS

FUNCTION	OPERATION	PATCHING
Operational Amplifier (with electronic switch and resistor feedbacks)	 $Eo = -\frac{R2}{R1}$ when Q = 0 $Eo = -\frac{R4}{R3}$ when Q = 1	
Summer (with use of the IC resistor network)	 Eo = -(A + B + C) NO PATCHING TO SWITCH CONTROLS "OP" OR "HD"	
Summer	 Eo = -(A + .1B)	
Integrator	 $Eo = -[T \int (A + B)dt + C]$ Initial condition mode when Q1 = 0 Operate mode when Q1 = 1 Hold mode when Q1 - 1 and Q2 - 1 With a 1 resistor and B capacitor: T = 1 sec/slow time; 2.5 ms/fast time.	

FUNCTION	OPERATION	PATCHING
MDAC	 Eo = K*Ein Where K is the digital data word attenuation factor.	
D/A Switch	 Eo = -(Rf/Rda)Ein when Q = 0 Eo = 0 when Q = 1 (Rda equals a "1" resistor)	
Comparator	 Q = 1 when Ein > Eb Q = 0 when Ein < Eb Control Panel Adjustment	
Nand Gate	 A B Q 0 0 1 1 0 1 0 1 1 1 1 0	
Nor Gate	 A B Q 0 0 1 1 0 0 0 1 0 1 1 0	
Monostable	 Approximately 100 us	
Divide by "N" Counter		

933.4 MODE CONTROL AND TIME BASE ASSEMBLY

Mode control is a push button, four stage, two pole, double throw interlocked switch. Each station places a system into one of four integrator modes:

Initial Condition (IC)

Hold (HD)

Operate (OP)

Repetitive Operation (RO)

To produce the above modes, it is necessary to control the OP Bus voltage (mode logic,) the Time Scale Relay Bus (slow or fast integrator time scales,) and the repetitive operation timing circuit (slow or fast time base ramp.)

Referring to the circuit diagram, the following is a description of the four modes:

Initial Condition...Time Scale Relay Bus energized (see Repetitive Operation.) The OP Bus pulled to ground.

Hold...Time Scale Relay Bus energized. The OP Bus pulled to the hold voltage state (approximately -1.7v.) Input to the time base integrator disconnected (see Time Base Circuits.)

Operate...Time Scale Relay Bus energized. The OP Bus released to the operate voltage state (less than -5v.)

Repetitive Operation...Time Scale Relay Bus de-energized. The OP Bus switched from the slow time modes (IC, HD, OP) to the repetitive operation logic.

Time Base Circuits...The time base integrator (amplifier B) provides both the slow and high speed repetitive operation time bases, both linear sweeps from negative to positive 10v reference. The input originates from amplifier A which is externally programmed to provide an adjustable voltage in the range of -1v to -10v. (A 1 volt input produces a compute time period of 100 sec; a -10v input produces 10 sec. The time base integrator circuit is the same as that of the 911 general purpose integrator. Please see the 911 data sheet for the circuit description.) When OP is depressed, the output of A is directed through the HD switch to R22 to produce an integration rate of 2 volts/sec; when RO Is depressed the input is R23 and the rate is 800 volts/sec. Also, when RO is depressed the monostable circuit of amplifiers C and D becomes the OP Bus and thus the repetitive operation mode control, (the time constant of C4-R18 producing an initial condition state of approximately 2 milliseconds.)

Capacitors C1 and C2 with resistors R1 and R2 decouple amplifiers C and D to eliminate power supply disturbance.

For the amplifier A Compute Time Period programming, please refer to section 2.0 of the GP-6 operator's manual.

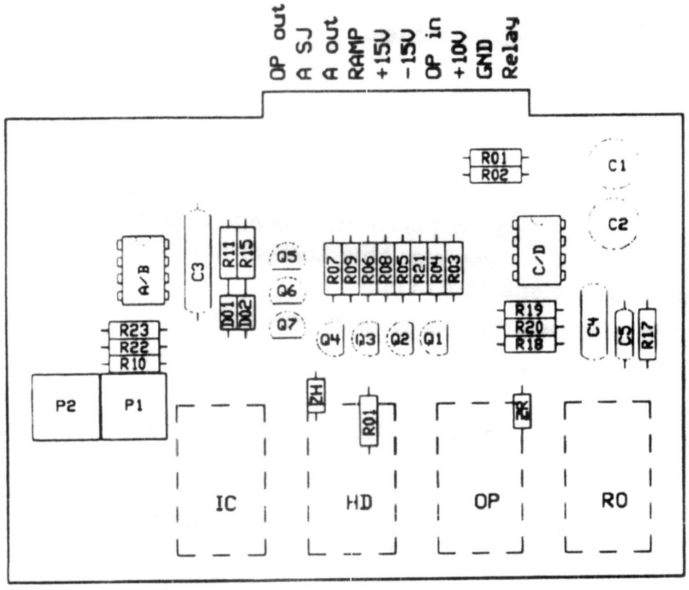
Adjustments

Slow time and repetitive operation time base rates are adjusted with potentiometers P1 and P2. Both are adjusted to match patch panel integrator time constants.

Program a patch panel amplifier as an integrator. Apply positive reference as an initial condition. Patch negative reference to a coefficient potentiometer and patch the wiper to a gain 1 input. Set the potentiometer to .200. The integrator will then sweep from negative to positive reference in a 10 unit (second) period.

Slow Time Adjustment...Observe (with an XY recorder or oscilloscope) the slow time output of the patch panel integrator as a function of the time base. Adjusts potentiometer P1 until the function passes through the positive reference-positive reference coordinate (+10, +10.)

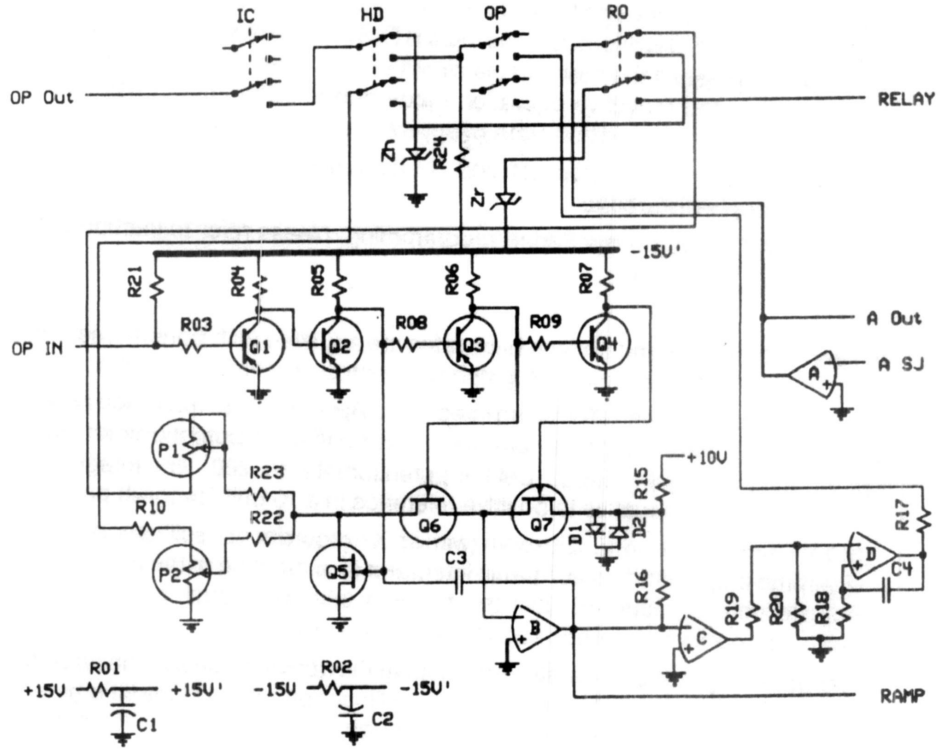
Repetitive Operation Adjustment...Repeat the above procedure observing the entire integrator output on the X-Y oscilloscope. Adjust potentiometer P2 until the oscilloscope trace passes through the +10, +10 coordinate.



Parts List

R1,2	100	ohm	
R17	1	K	
R20,24	4.7	K	
R15,16	10.0	K*	
R4-7	15	K	
R21	27	K	
R3,8,9,19 . . .	47	K	
R10	100	K	
R18	330	K	
R22	1.0	K*	
P2	5	K	
P1	50	K	
C1,2	33	ufd	electrolytic
C3	1	ufd	polycarbonate
C4	.022	ufd	mylar
C5	3500	pf	mylar
D1,2	1N4148		
ZH	1N4370		
ZR	1N5231		
Q1-4	2N4403		
Q5-7	2N5485		
A/D	TL082CP		
C/D	Mc1458		

Schematic



905.4 DIGITAL VOLTMETER

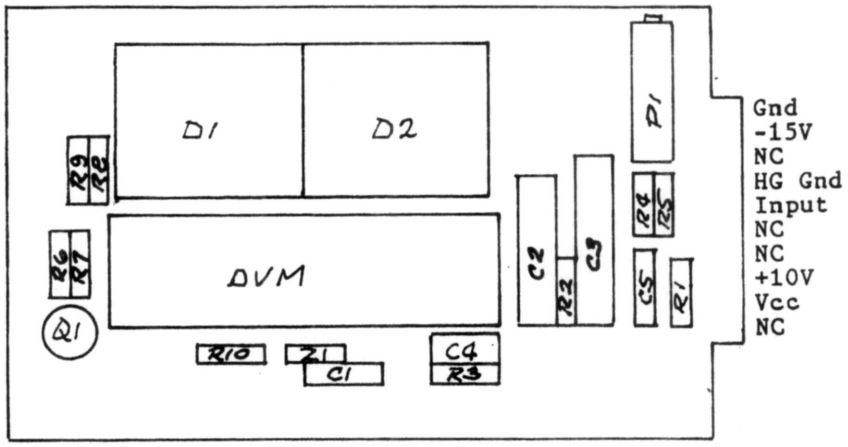
The 905 assembly Is a digital voltmeter that functions as a ratioraeter of input voltage signals to computer reference. The full scale 1.000 reading is a unity ratio of the input reference value. For normal operation, the 1.000 reading is equivalent to 10.00 volts.

All active circuitry is contained within the Intersil 7107 component. For a description of the circuit functions, please refer to Intersil data sheet 11-77-00B.

Adjustment

The single adjustment should be trimmed so that the display shows +1.000 display when the input is +10 reference.

Assembly Drawing

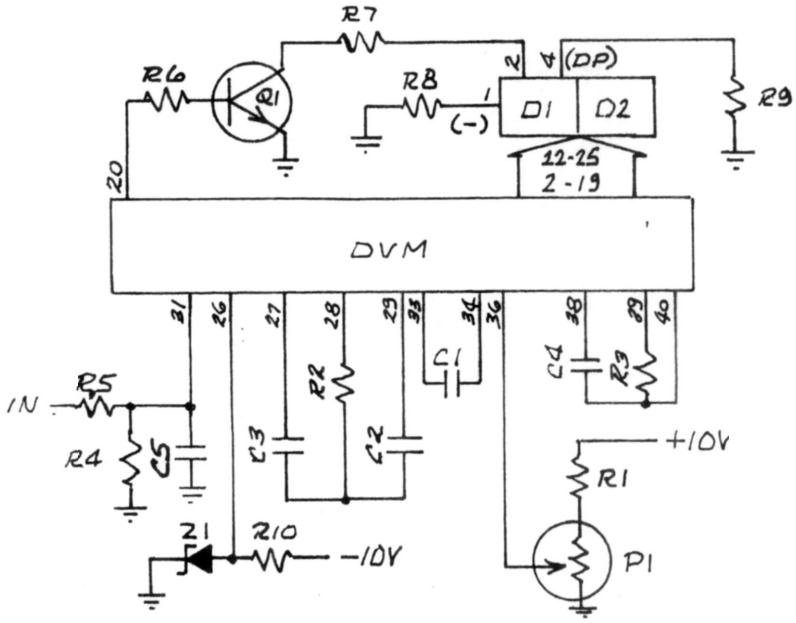


Parts List

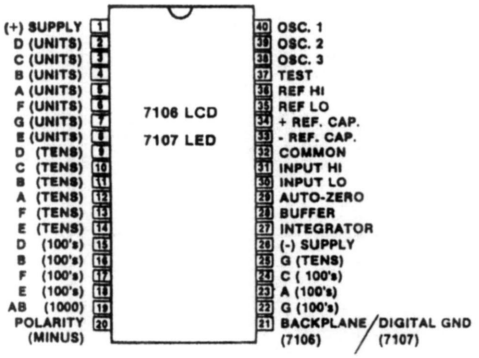
R7-9	180	
R10	4.7	K
R6	15	K
R2	47	K
R1	49.9	K*
R3	100	K
R4	100	K*
R5	1	M*
P1	10	K
C4	100	pf
C5	.01	ufd
C1,C6	.1	ufd
C3	.22	ufd
C2	.47	ufd
Z1	1N5231	
Q1	2N4124	
DVM	ICL7107CPL	
D1	MAN 6730	
D2	MAN 6710	

*1% metal film resistor

Schematic



7107 Pin Configuration



7913.1 REGULATOR

The 7913 Regulator provides the unregulated supplies +UN and -UN from the 28 volt CT transformer. Regulated plus/minus. 15 volts, precision plus/minus 10 volts reference and Vcc (plus 5 volts) are also provided.

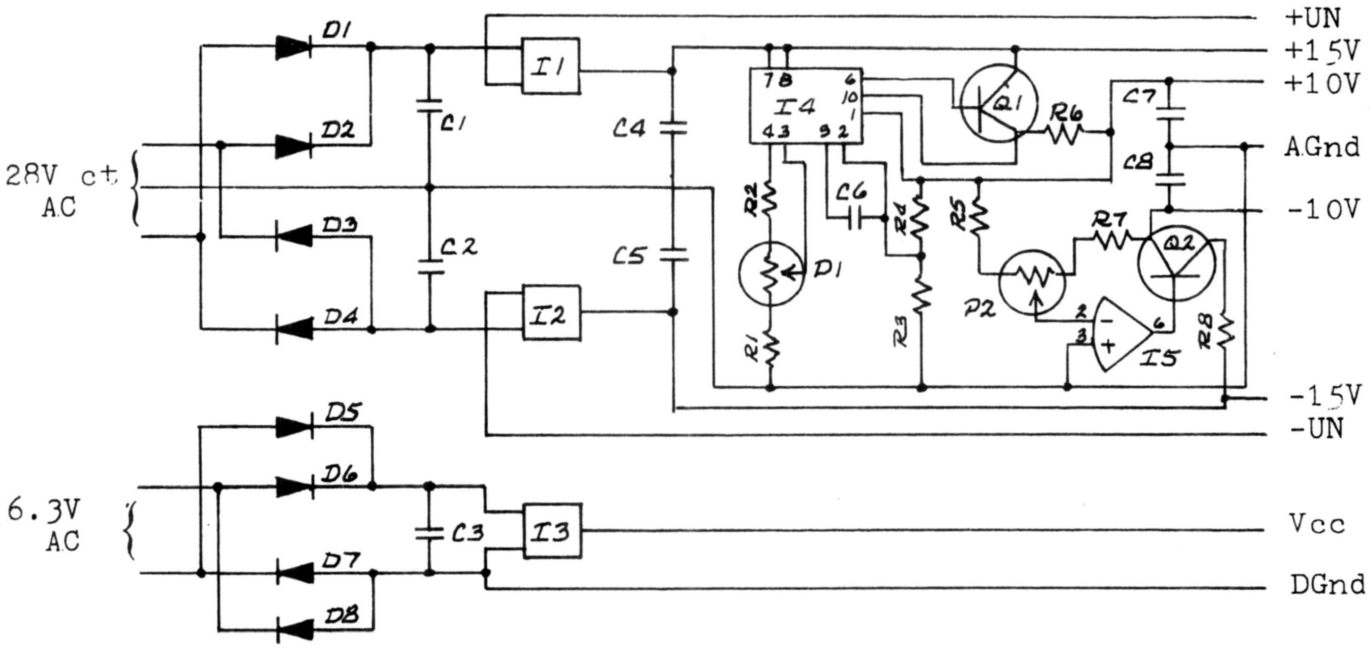
The precision positive 10 volts reference is produced by regulator I4. Negative tracking 10 volts reference is produced by inverting amplifier I5.

Reference Adjustments

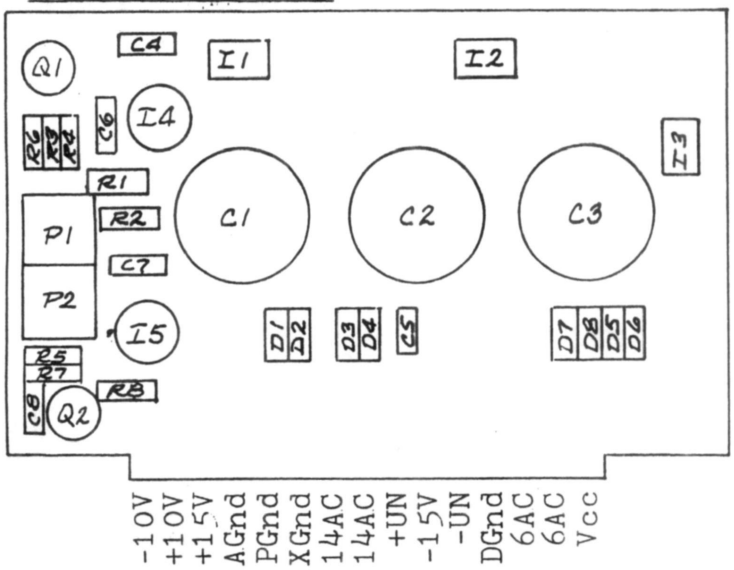
1. Adjust potentiometer P1 until the positive reference is +10.000.

2. Adjust potentiometer P2 until the negative reference is -10.000.

Circuit Schematic



Assembly Drawing



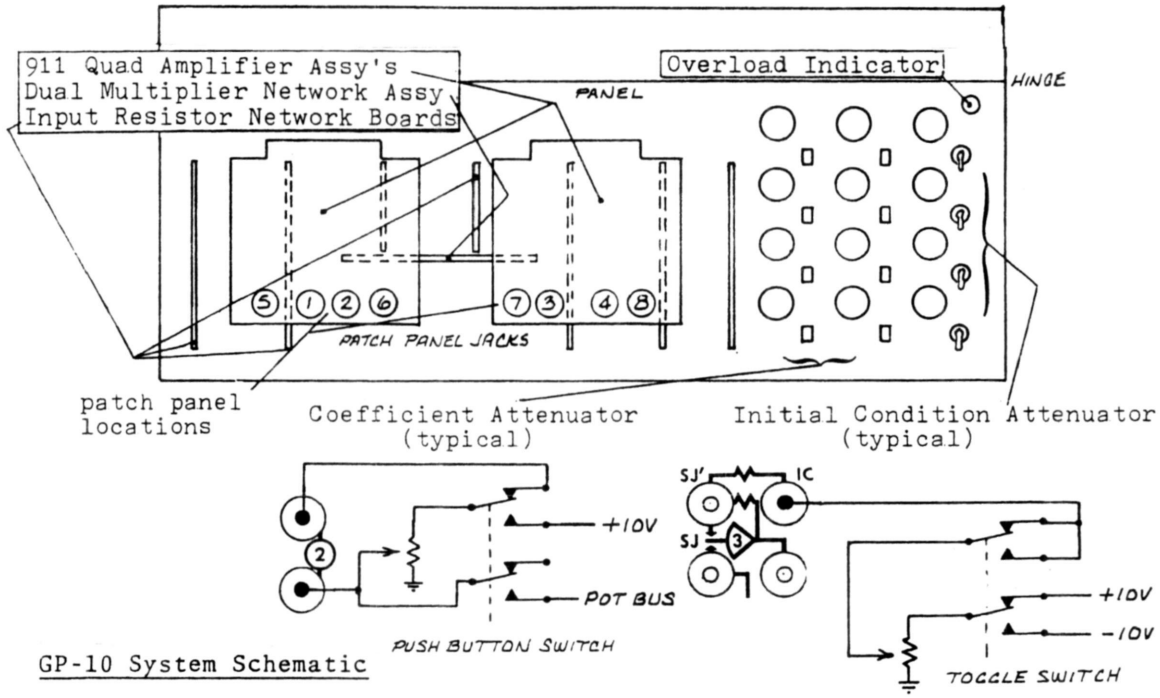
Parts List

R6,R8	10 ohm
R2	2.32K#*
R3	2.43K#
R5,R7	4.99K#
R1	6.04K#
R4	9.76K#
P1,P2	50 ohm
D1-D4	1N5401
D5-D8	1N4001
Q1	2N4124
Q2	2N5138
I1	UA7815
I2	UA7915
I3	UA7805
I4	UA723
I5	MC1741CG

* value may be altered
\# metal film resistor

GP-10 COMPUTING UNIT

The GP-10 computing unit performs the functions that are outlined by the patch panel layout of page 21 through use of the assemblies shown in the GP-10 system schematic.



GP-10 System Schematic

911 Quad Amplifier Assembly...Two identical PCB assemblies provide the eight patch panel amplifiers. Patch panel locations are shown on the GP-10 system schematic.

Input Resistor Network Boards...Amplifiers 1-6 have individual boards that connect the 50K and 5K patch panel input resistors. (It is noted that all 50K resistors have a 15K resistor from the input jack to ground. These resistors help to keep summing junction loading somewhat constant and thus minimize the effects of varying input loads. The 33pf compensation capacitor found on each summer-integrator board is placed across the SJ' feedback resistor.)

Integrator Initial Condition Attenuators...Amplifiers 1-4 have individual attenuators that are provided to enter integrator initial conditions. As shown on the typical circuit, each has a DPDT CO toggle switch that allows an operator to apply positive and negative initial conditions or to disconnect the attenuator.

Dual Multiplier Network...The multiplier network PCB plugs into the 10 pin connector, as shown on the GP-10 system schematic, with the components facing the top of the panel so that when the panel is in an open condition there is access to the adjustment potentiometers.

External Function Generators...Function generator input jacks are provided amplifiers 7 and 8 as shown on the patch panel layout. The jacks do not have standard connections.

Coefficient Attenuators...The eight coefficient potentiometers are located on the panel as shown on the GP-10 system schematic. Each has a push button coefficient setting switch that, when depressed, replaces the patch panel input with reference and connects the wiper to the Pot Bus.

Mode Control...Logic control found at the OP patch panel jacks is the system OP Bus. (See para 2.3)

Reference...Plus and minus 10 volts.

Trunks...The eight patch panel TRUNKS are terminated at one of two data connectors. (See para 2.9.2)

911-3 QUAD AMPLIFIER ASSEMBLY

The 911 board provides two single input, high gain operational amplifiers and two high gain operational amplifiers with electronic switch/integrator networks.

Amplifiers A and D are the single input amplifiers. Their patch panel summing junctions are connected directly to the inverting bases. Back-to-back diodes D2 and D3 offer protection by limiting summing junction potential. Capacitor C1 reduces peaking.

Amplifiers B and C are single input amplifiers with electronic switch/integrator networks. The electronic switches create two summing junctions, SJ and SJ'. When the switch control input (OP) is a logic 0 (ground or positive) summing junction SJ' conducts; when a logic 1 (more negative than -5 volts) summing junction SJ conducts.

The integrating capacitors are connected to the SJ summing junction so that an integrator is programmed by patching an amplifier output to a capacitor input. Two capacitor inputs (B and .1B) offer 10:1 time scale selection. The Time Scale Relay switches the time scale change (400:1) that is required for high speed repetitive operation. Where the repetitive operation feature is provided, the repetitive operation capacitors are connected directly to SJ. When the relay is energized, slow time capacitors are switched parallel the repetitive operation capacitors. (The relay is energized when an approximate negative 10 volts, not negative reference, is applied to the relay control input.)

Signal switching is performed by N-channel FET transistors Q6 thru Q8. Bipolar transistors Q1 thru Q5 are the FET switch drivers. Q6 is the Hold FET (it's on resistance is less than 30 ohms to minimize summing errors.) Voltage divider resistors R8 and R12 are selected so that when OP is between -1 to -3 volts, Q6 shuts off; when OP is more negative Q6 turns on. Q7 is the shunt switch, Q8 is the SJ series switch and Q9 is the SJ' series switch. Table 5-1 shows the switch states for the OP logic control voltage levels. N-channel FETs conduct with a zero gate voltage and shut off with approximately -7 volts. Back-to-back diodes D4 and D5 limit the SJ' potential when Q9 is off. Diodes D2 and D3 provide summing junction protection. D1 allows the Hold Inhibit control to override Q1 and turn Q6 on. (Hold Inhibit logic is applied in the Pot Set Mode to ground SJ summing junctions that would otherwise be floating.)

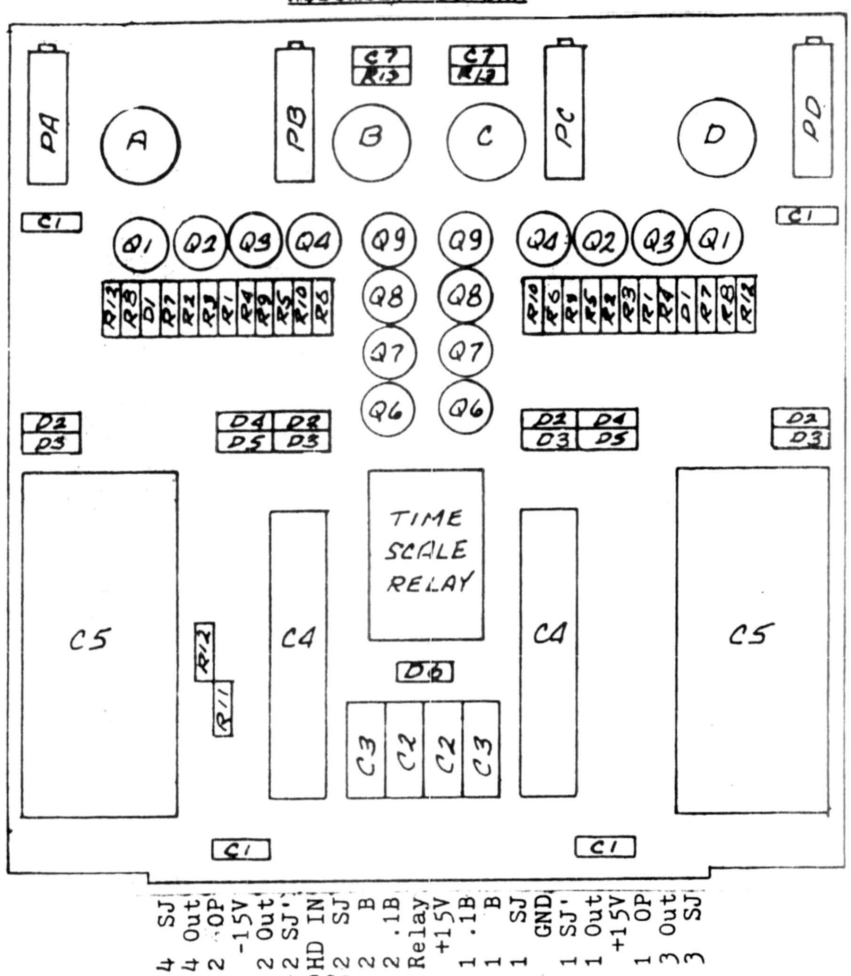
Capacitors C7 and resistors R13 provide amplifier compensation. Capacitorss C1 reduces peaking when SJ has a resistor feedback. A similar capacitor is provided the SJ' summing junction.

BALANCING

To balance amplifiers A and D, patch resistor feedbacks and adjust potentiometers PA and PD until each amplifier output is a zero potential.

Amplifiers B and C should be balanced when programmed as integrators. Adjust PB and BC until each integrator produces a minimum integrator drift.

Assembly Drawing



Parts List

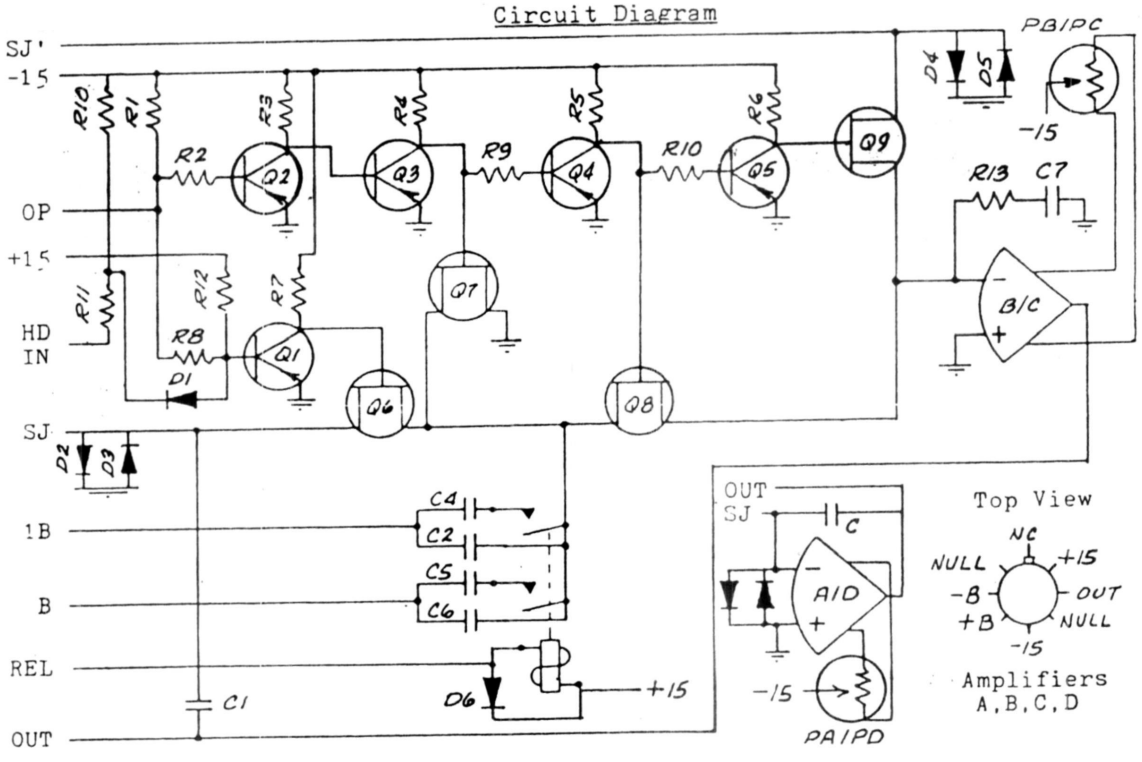
R13	1 K*
R11	2.2 K
R2-R7	15 K
R1, R10	27 K
R8-R10	47 K
R12	330 K
PA, PB, PC, PD	10 K
C1	15 pf
C2	.005 uf
C3	.05 uf
C4	2 uf
C5	20 uf
C7	500 pf
Q1-Q5	2N5138
Q6	2N4091
Q7-Q9	2N5163
Amplifiers A, D	MC1741CG
Amplifiers B, C	LH0042CH
Relay 1	4A, 24V

Table 5-1

OP LOGIC	Q6	Q7	Q8	Q9
OP ≥ 0	OFF	ON	OFF	ON
-1V > OP > -3V	OFF	OFF	ON	OFF
OP -5V	ON	OFF	ON	OFF

Note: When HD IN (Hold Inhibit) <-1V, Q6 remains ON.

Circuit Diagram



970-1 OVERLOAD INDICATOR

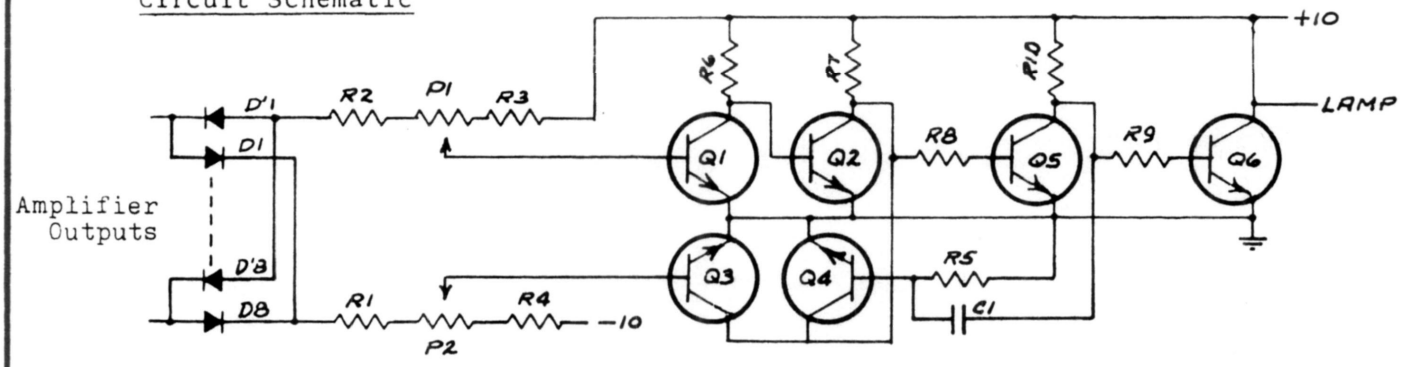
The 970-1 Overload Indicator compares eight amplifier outputs with positive and negative 10 volts reference. When any output exceeds reference a lamp driver conducts.

When a negative overload occurs Q1 shuts off and Q2 conducts. When a positive overload occurs Q3 is turned on, pulling Q2 to an on condition. Positive 15 volts through an incandescent lamp is pulled to ground when Q6 conducts. Resistor R5, capacitor C1 and Q4 provide a temporary latch so that momentary overload outputs are observed by the lamp indicator.

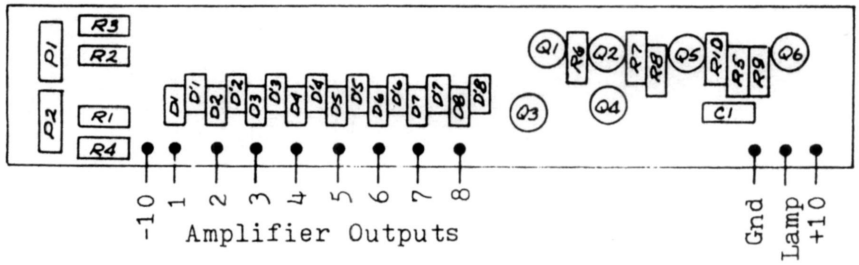
Adjustments

Apply a +10.5 volt level to any amplifier output. (10.5 volts provides a .5 volt overrange.) Adjust potentiometer P2 until the lamp indicator turns on. Apply a -10.5 volt level and adjust P1.

Circuit Schematic



Assembly Drawing



Parts List

R1 thru R4,R6,R7,R10	15 K
R8,R9	4.7 K
R5	27 K
C1	6.8 ufd
P1,P2	5 K
Q1 thru Q6	2N5132
Diodes	1N4148

982.1 DUAL MULTIPLIER NETWORK

The 982 assembly provides two independent multiplier networks, configured so that each, when used with an external operational amplifier, may be programmed as a multiplier, divider, squarer and square rooter.

Two inputs (Xin and Yin) are multiplied by integrated circuit IC to produce a voltage proportional to the product X*Y. The voltage is converted to a current by resistor R1. The current source SJ is scaled so that when it is connected to the summing junction of an operational amplifier for operation as a multilier, and where the amplifier's feedback is a 50K ohm feedback resistor, the amplifier output will produce a full scale 10 volts when the X and Y inputs are 10 volts.

Adjustments...Each network is originally adjusted at the factory. The networks should, however, be checked and readjusted, if necessary, during the initial checkout. Thereafter they should be periodically checked to assure their most accurate operation. About ten minutes system warmup should be allowed before making the adjustements.

Adjustments consist of a zero offset balancing and a trim for gain and linearity. The suggested procedures are offered as follows:

1. Program the network as a multiplier with a standard gain 1 (50K) feedback.

2. Patch inputs X and Y to ground. Adjust Pz for a zero output.

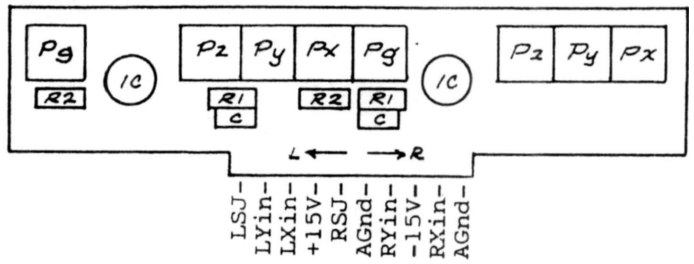
3. Program an integrator as a ramp to sweep from minus to plus reference. (For convenience make all adjustments in the repetitive operation mode with the oscilloscope readout.) Display the multiplier vs. ramp outputs. Patch the ramp to the Y input; the X input should remain patched to ground. Adjust potentiometer Px until a best zero curve is displayed.

4. Reverse the X and Y inputs. Adjust Py until a best zero curve is displayed.

5. Readjust Pz if necessary.

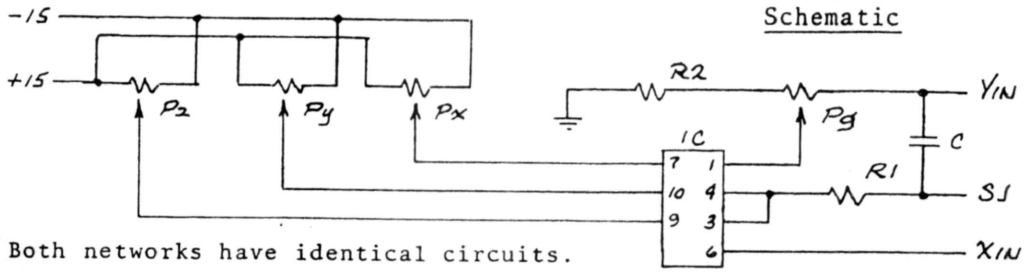
6. Patch reference to the X input and the ramp to Y. Sum the multiplier output with the correct ramp polarity so that an error curve is displayed. Adjust Pg until a best curve is obtained. Reverse X and Y and check the curve. Reverse the reference input polarity (also the summed ramp polarity,) check both combinations of X and Y inputs, and compare with their opposite polarity counterparts. Adjust Pg until a best combination of the four error curves is displayed.

Assembly Drawing



Parts List

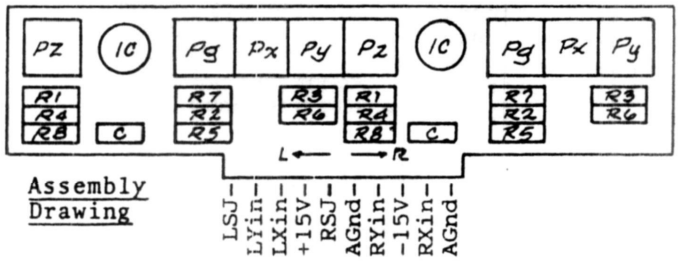
R1	49.9	K
R2	10.0	K
C	33	pf
Pg	5	K
Pz,Px,Py	20	K
IC	ICL8013BCTZ	(standard)
	ICL8013ACTZ	(medium)



Both networks have identical circuits.

983 DUAL MULTIPLIER NETWORK (high accuracy)

The 983 circuit is functionally the same as the 982. Please refer to the 982 data sheet for operating and adjustment procedures.

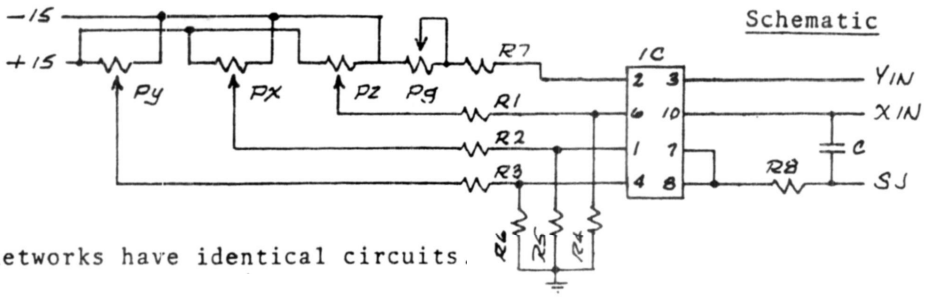


Assembly Drawing

Parts List

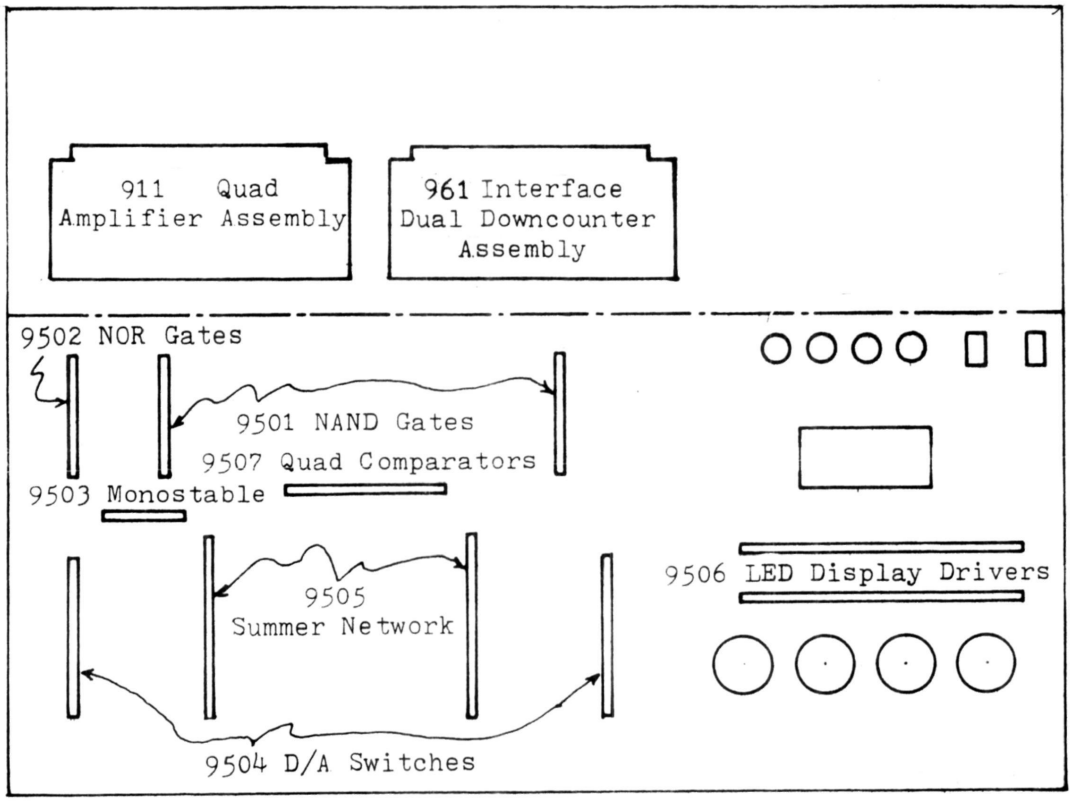
R1,2,3,7	470 K
R4,5,6	1 K
R8	49.9K
Pg	1 K
Pz,Px,Py	50 K
C	33 pf
IC	AD534LH

Schematic



Both networks have identical circuits.

MICROHYBRID I SYSTEM LAYOUT



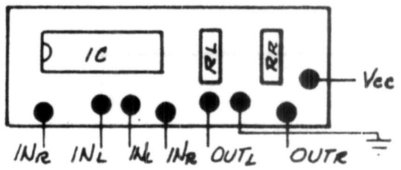
The above system layout shows locations of Microhybrid printed circuit assemblies. See individual data sheets for wire list connector terminations.

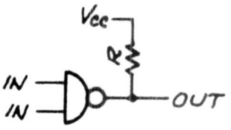
System Parts List

Patch Panel Jacks - EF Johnson 108-09xx-001
Comparator Bias Potentiometers - C.T.S. VA 45D 5K
Toggle Switch - MST 105D
Red Pushbutton - Switchcraft DA-01-3
Black Pushbutton - Switchcraft DA-02-3
Orange LED - Monsanto M5152
Green LED - Monsanto M5252
Yellow LED - Monsanto M5352
Red LED - Monsanto MV5752

MICROHYBRID PANEL MOUNTED CIRCUIT BOARD ASSEMBLIES

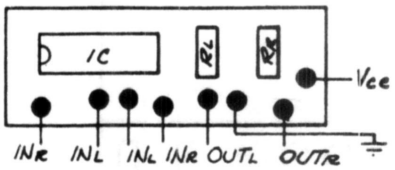
NAND GATES, Dwg 9501

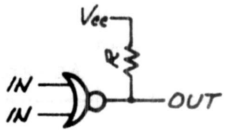




R	4.7 K
IC	74LS03

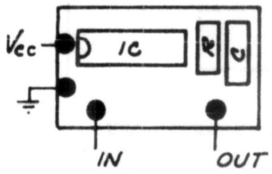
NOR GATES, Dwg 9502

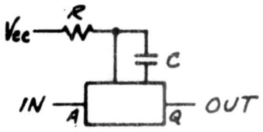




R	4.7 K
IC	74LS33

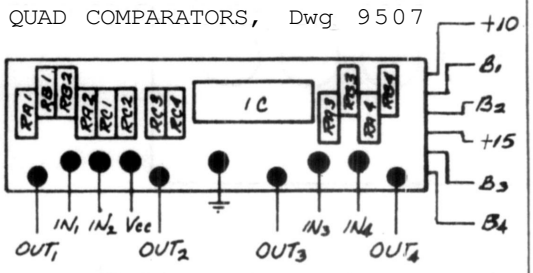
MONOSTABLE, Dwg 9503

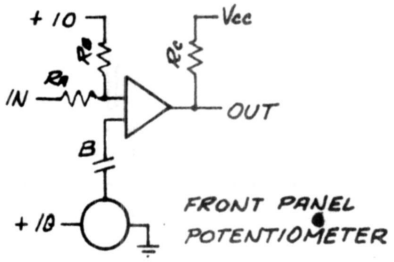




R	47 K
C	2700 pfd
IC	74121

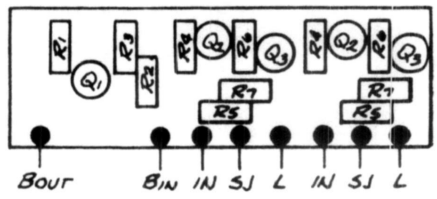
QUAD COMPARATORS, Dwg 9507

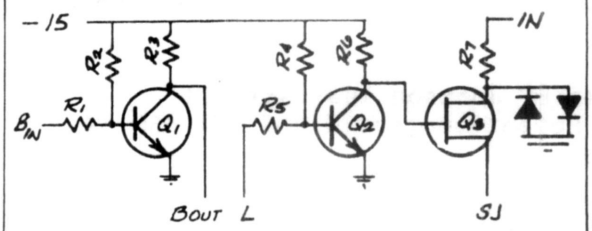




RA,RB	4.99K
RC	4.7 K
IC	MC3302

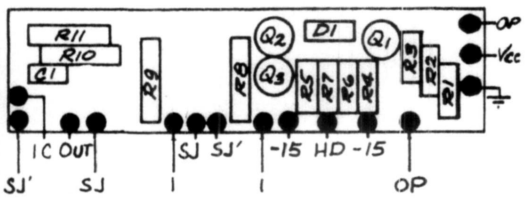
D/A SWITCHES & BUFFER, Dwg 9504

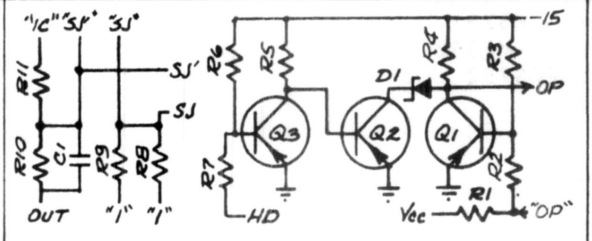




R1,R3,R5,R6	15 K
R2,R4	100 K
R7	49.9 K
Q1,Q2	2N5138
Q3	2N5163
Diodes	1N4148

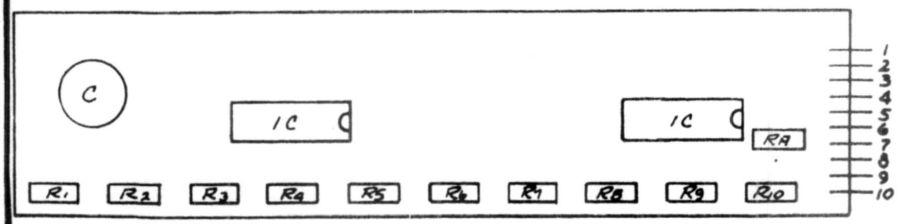
INPUT NETWORK, Dwg 9505

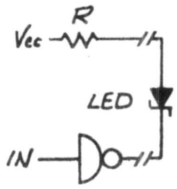




R2,R4,R5,R7	15 K
R1	27 K
R3,R6	100 K
R8-R11	50.0 K
C1	15 pfd
Q1-Q3	2N5138
Zener	1N5227

LED DISPLAY DRIVERS, Dwg. 9506





RA	100
R1-R10	1 K
C	25 ufd
IC	74LS05

761 INTERFACE AND DOWNCOUNTER BOARD

1.0 The following circuits comprise the board:

Mode Indicators...Analog Mode Control/TTL Patch Panel Output
Mode Control...Patch Panel Output TTL/Analog Mode Control
Patch Panel Relay Drive Control
Compute Time Clock
Dual Downcounter

1.1 Mode Indicators

The analog computer mode control (OPAD) originating at the 933.4 Time Base Assembly is buffered to produce TTL outputs OPOP and HDOP.

An OPAD initial condition state (> 0) produces an OPOP low.
An OPAD operate or hold state (< 0) produces an OPOP high.
An OPAD hold or IC state (> -3V) produces an HDOP high.

1.2 Mode Control

Mode control originating at the Microhybrid I patch panel (OPIP and HDIP) is buffered to produce the system OP bus (OPDA.)

A OPIP low produces an OPDA initial condition state (0.)
A OPIP high produces an OPDA operate state (< -3V.)
When OPIP is high, HDIP high pulls the OPDA bus to approximately -2v.

1.3 Patch Panel Relay Drive Control

The connector termination TRSD is connected to the time scale relay bus. System relays have their coils connected to +15v and the TSRD bus. Zener Z2 provides a 5.1v drop between the +15v and -15v sources. A high or absence of a TSPP patch panel input will activate the relay bus (slow time capacitors) and enable normal system control; a low will disable system control, forcing a deactive state (fast time capacitors.)

1.4 Compute Time Clock

Compute Time clock pulses of .1 sec as referred to the fast time scale (CTC) are terminated at patch panel CLK. Pulses begin and continue to run when the OP patch panel mode control (OPOP) goes and remains high. CLK is held low when OPOP is low. A high/low pulse transition is the end of a period.

1.4.1 Adjustment... The compute time clock is adjusted by potentiometer P1. The following are suggested adjustment procedures.

1. Set the compute time period to 10 sec and place the unit into the RO mode.
2. Patch CLK to the R downcounter input.
3. Set the downcounter to 10 counts.
4. Display on the oscilloscope the downcounter output as a function of TIME.
5. Adjust P1 until the tenth pulse appears at the full scale X axis co-ordinate.

1.5 Dual Downcounter

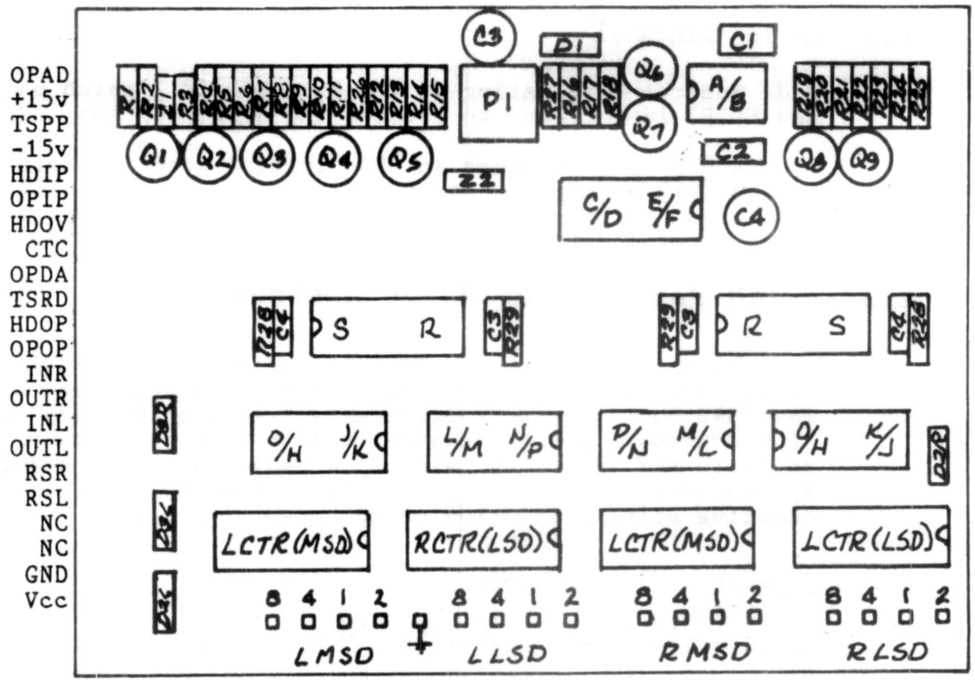
The L and R downcounters deploy identical circuits.

A high/low input triggers monostable R which provides a pulse to the downcount input of CTR(LSD.) Is borrow output is connected to the downcount input of CTR(MSD.)

BCD thumbwheel switches pull preset inputs to ground, thereby resetting the counters to thumbwheel settings. When the outputs of both CTR(LSD) and CTR(MSD) are zero, NOR gates L,M,N,P are high. The high/low transient of gate K triggers monostable S and thereby resets the counters. The pulse also sets a S-R latch programed from gates H/J. The patch panel output (OUT) thus remains high until the next input resets the latch.

An RS input low presets the counter to the thumbwheel setting. The L counter receives the preset from patch panel RS; the R counter from the patch panel mode control OPOP. Thus, the L counter requires preset patching while the R counter will only preset while in the initial condition mode.

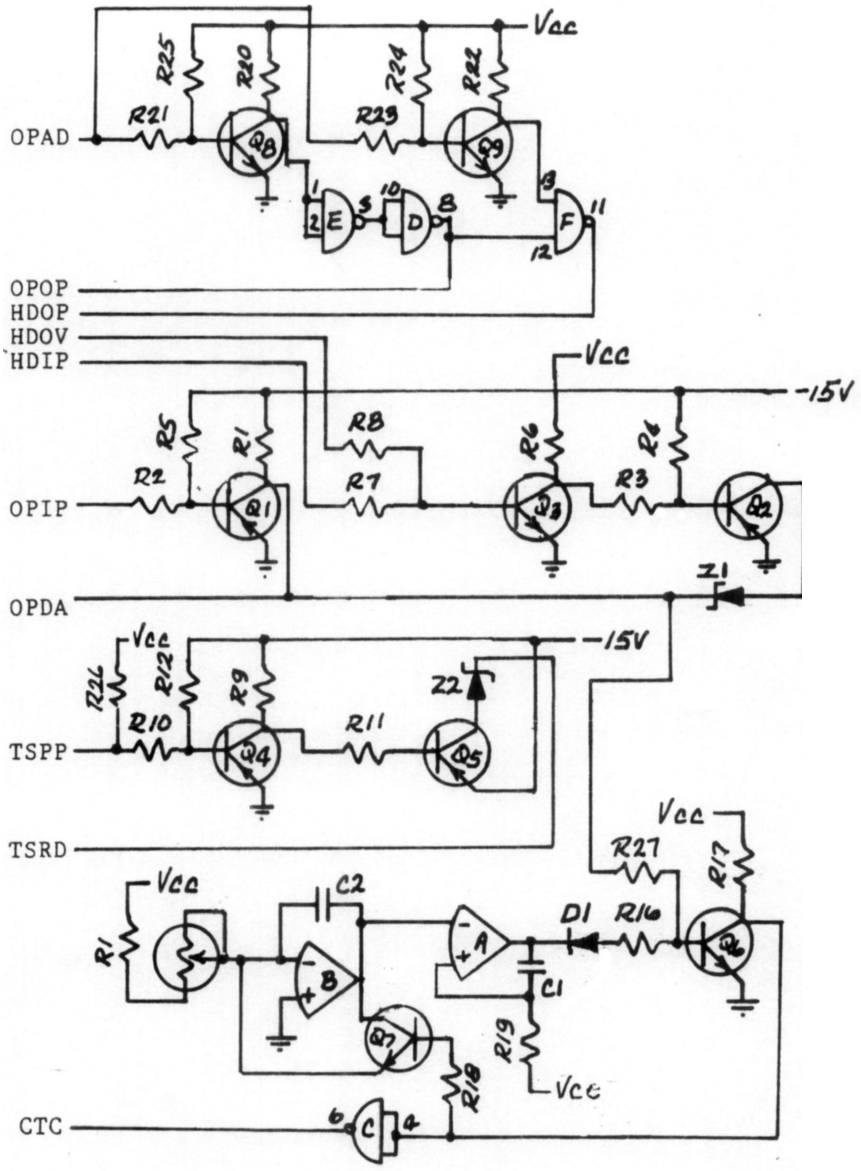
Assembly Drawing

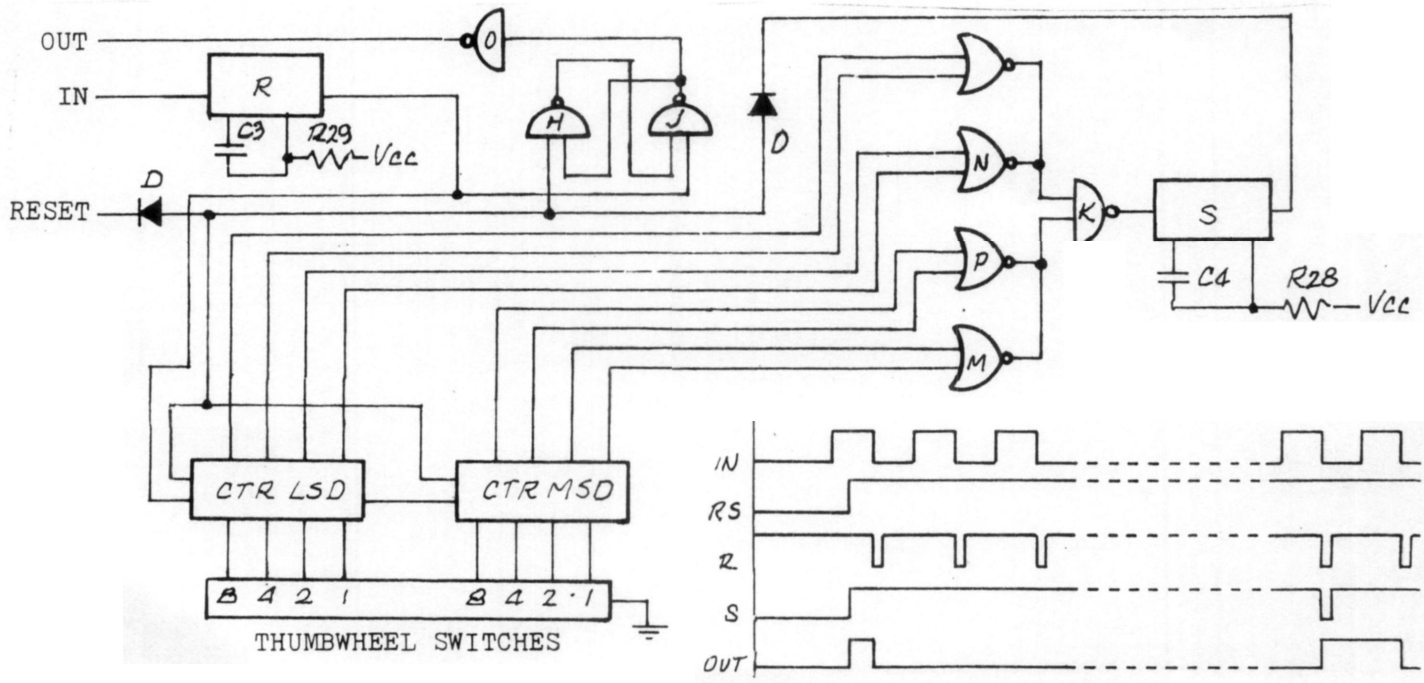


Parts List

R13,14	10	ohm		D1-D3	1N4148
R9,28,29	4.7	K		Z1	1.75v zener
R15	4.99	K*		Z2	5.1v zener
R1-3,6-8,10,11, 16-18,20-22,26	15	K		Q1,2,4	2N4403
R23	18	K		Q3,6-9	2N4124
R19,24	22	K		Q5	MPS A13
R25	47	K			
R4,5,12,27	100	K		A/B	MC1458
P1	5	K		ABCD,OHJK	74LS00
				LMNP	74LS33
C3,C4	560	pf cer		CTR	74LS192
C1	3300	pf cer			
C2	.02	uf myl			

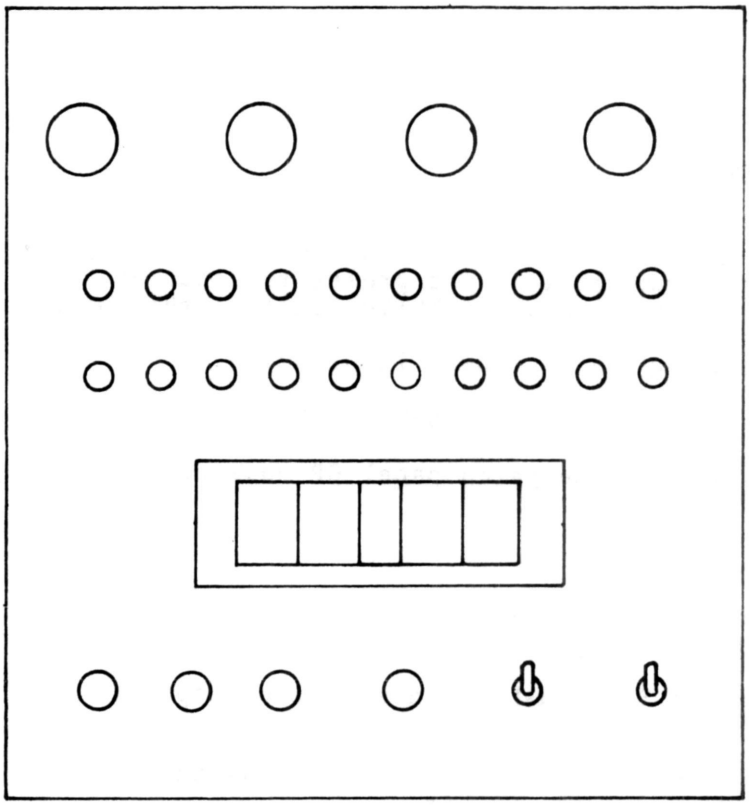
Schematic





Timing Diagram

3.0 CONTROL PANEL OPERATIONS



3.1 COMPARATOR BIAS ADJUSTMENTS

3.2 LED INDICATORS

3.3 DIVIDE BY "N" COUNTER PRESET SWITCHES

3.4 OPERATOR CONTROLS

3.1 COMPARATOR BIAS ADJUSTMENTS

Each of four Comparator Bias Adjustments (knobs k1 thru k4) produces a voltage level that is one of two inputs to a patch panel comparator. The second input is the patched analog variable. When the analog variable is more positive than the bias level, the comparator output is a logic 1; when it is more negative the output is a logic 0. Bias levels are adjustable through a range of -10 volts to +10 volts.

3.1.1 Bias level setting procedures.

a. Apply a constant voltage equal to the desired bias level as the patch panel comparator input.
b. Turn the Comparator Bias Adjustment knob until a comparator state change is observed. To reach the transient position...
   - If the output is a logic 0, turn the knob counterclockwise.
   - If the output is a logic 1, turn the knob clockwise.

3.2 LED INDICATORS

3.2.1 Comparator Indicators...An LED is lit when a comparator output is a logic 1.

3.2.2 Gate Indicators...An LED is lit when a gate output is a logic 1.

3.2.3 I/O Bus Indicators...An LED is lit when an I/O Bus patch panel input is a logic 1. To be a logic 1, the I/O bit must be latched high by a digital computer IOW command. So latched, the bit may then be pulled low by a patched logic operation.

3.2.4 Stop...The STOP LED is lit while the digital computer RDY command is in effect. Depressing the STOP pushbutton does not light the LED.

3.2.5 Go...The GO LED is lit while the Go status bit is a logic 1.

3.3 DIVIDE BY "N" COUNTER PRESET

Thumbwheel switches produce preset logic for the two divide by "N" BCD two decade downcounters. The left hand thumbwheel is the preset for patch panel counter "L"; the right hand thumbwheel is the preset for counter "R". Each counts the trailing edges of input pulses. While counting the output is a logic 0. When the counter register is zero, the output becomes a logic 1 and remains a logic 1 until the trailing edge of the next input pulse.

The L counter is preset when the "R" patch panel input is a logic 0.

The R counter is preset when the patch panel OP mode control input (blue jack) is a logic 0.

3.4 OPERATOR CONTROL SWITCHES

3.4.1 GO...Depression of the GO pushbutton sets the Go status bit, lights the GO LED and clears the Reset, Stop, Interrupt and Interrupt W/Hold status bits.

3.4.2 STOP...Depression of the STOP pushbutton sets the Stop bit, sets the Interrupt bit and clears the Go bit.

3.4.3 RESET...Depression of the RESET pushbutton sets the Reset status bit, sets the Interrupt bit and clears the Go bit.

3.4.4 Momentary Switch... While released, patch panel logic at the "M" switch jack is a logic 1. Depression of the momentary switch produces a logic 0.

3.4.5 Toggle Switch...The toggle switch position produces a logic 0 or 1 at the patch panel jack "T".

3.4.6 POWER...AC power is off when the toggle switch is in the down position and is on when the switch is in the up position.