7000 ANALOG/HYBRID COMPUTING SYSTEMS

Operators and Maintenance Manual

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APPENDICES

GENERAL SET UP

1.0 Connection of Analog Readout Instruments

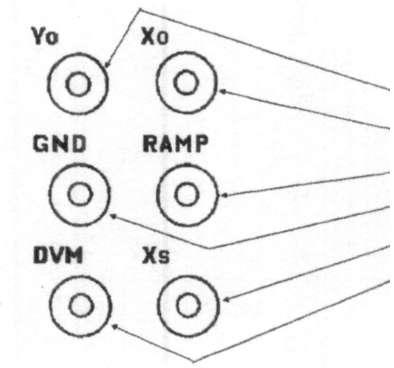
1.0 Oscilloscope and XY Recorder

A 7000 system operates In both manually controlled slow time and high speed repetitive operation. Readout features are provided for convenient use of a DC XY oscilloscope and XY recorder. The electronic address network enables a two channel oscilloscope to display and a two pen recorder to plot:

a. **Y vs. X** *where X and Y are keyboard selected computing unit amplifier outputs*

b. **Y, X vs time** *and time is the internal Time Base Ramp.*

fig. 1-0



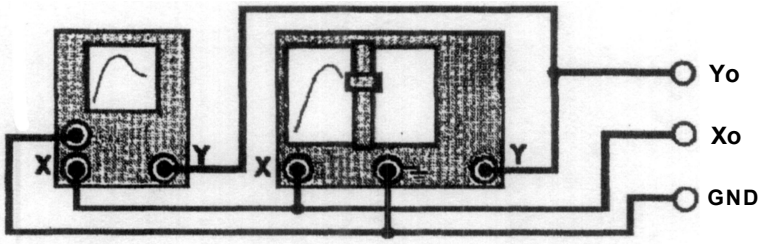
Y Address Amplifier Output
Operator selected X Address Amplifier Output or the Time Base Ramp
Time Base Ramp
Analog Ground
X Address Amplifier Output
Digital Voltmeter Input or Attenuator Setting Bus

Recommended connections are as follows (See para 2 . 2 for **Y** and X address procedures.):

1.1.1 **Y vs. X** or **Y vs. time** (single channel vertical input)

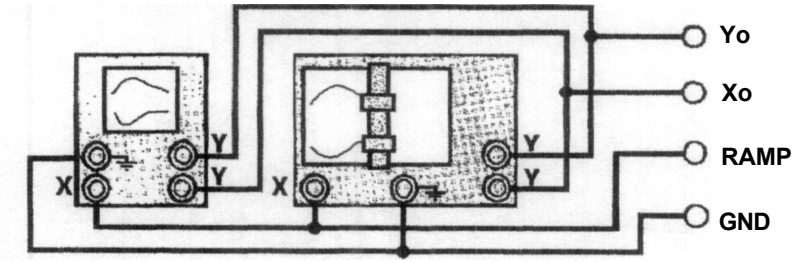
Y vs. time position the X Address toggle switch to TIME

Y vs. X position the X Address toggle switch to AMP.



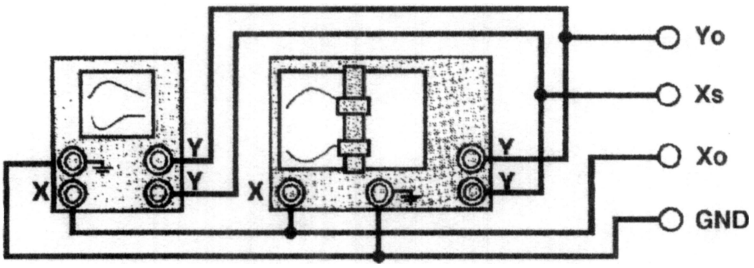
1.1.2 **Y, X vs. time** (Control Unit X amplifier selection)

-position the X Address toggle switch to AMP.



1.1.3 **Y, X vs. time** (Digital Computer X amplifier selection)

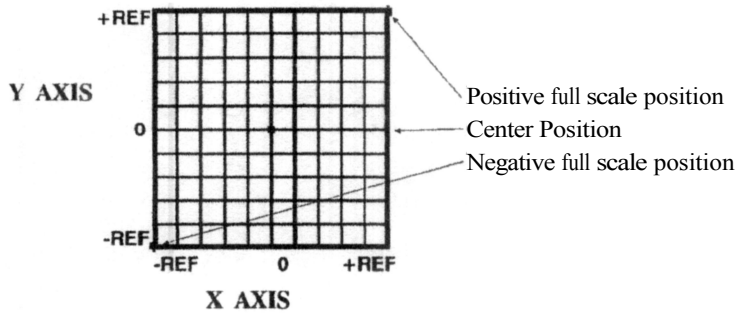
position the X Address toggle switch to TIME



1.1.4 **Calibration**

Both the oscilloscope and XY recorder are calibrated so that their full scale horizontal and vertical axes extend between negative and positive reference (minus and plus 10 volts) as shown in fig. 1-4.

The Xo and Yo outputs have associated toggle switches that are located on the Analog Output panel to provide convenient full scale X and Y axis calibration. When the toggle switches are in the center positions, the outputs are the X and Y address selections. When in the top and bottom positions, the outputs are positive and negative reference.



1.2 **Strip Chart Recorders**

Two inputs to a multi-channel strip chart recorder may be the X and Y address outputs. Other inputs to the recorder may be patched directly to the computing unit patch panel amplifier output jacks or indirectly through the computing unit trunk jacks and Trunk Connector.

1.3 **Digital Voltage Measurements**

1.3.1 **Control Unit**

A 3 1/2 place accuracy, autopolarity digital voltmeter is available for measurements of attenuator settings, amplifier outputs and external voltage inputs.

The display decimal point is positioned for normalized analog computer scaled variables: 10 volts reference is displayed as unity, +/-1.000. Actual measured voltages are thus 10 times their displayed values.

Calibration ...A full scale calibration potentiometer is located within the Control Unit. To perform an adjustment, position the analog output panel DVM toggle switch to "+" and trim until a 1.000 reading is observed.

1.3.2 External **DVM**

An external digital voltmeter may be connected to perform the same measurements as above.

Amplifier Outputs ...Connect to either the Amplifier Output Panel, Yo or Xo jacks.

Attenuator Settings... Connect to the Amplifier Output Panel, DVM jack.

OPERATOR PROCEDURES

2.1 Digital Voltmeter Measurements

2.1.1 Setting Coefficient Attenuators

1. Make sure the Amplifier Output panel POT is in the center position.
2. Place the system into the IC mode.
3. Position the DVM toggle switch to POT.
4. Depress the Attenuator Set-up button adjacent to the attenuator to be set; adjust the attenuator until the DVM displays the desire setting.

2.1.2 Measurement of Static Amplifier Outputs

1. Place the DVM toggle switch to AMP.
2. Place the X Address toggle switch to AMP.
3. The DVM measures the amplifier output selected by the X address.

2.1.3. Measurement of the Sum of Integrator Inputs

1. Place the system into the IC, then HD modes. *Only the HD LED should be lit.*
2. Patch the SJ jack of the integrator whose input is to be measured to the SJ jack of an unused amplifier.

   *The amplifier is to be a summer with a normal 1 resistor feedback. **

3. Measure the amplifier output. It is the inverted sum of the integrator inputs.

   *If the sum produces an overrange, reduce the amplifier feedback to a .1 resistor.

2.1.4 Measurement of External Inputs

1. Connect the input to be measured to the DVM jack at the Analog Output panel.*
2. Position the DVM toggle switch to POT.
3. The DVM display is the measurement.

   **Remove the input prior to a next coefficient attenuator setting.*

2.2 Amplifier Selection

2.2.1 Y Address

1. Depress the red Y key.
2. Depress a 0 thru 7 white key to address the sector (computing unit number.)
3. Depress a 1 thru 8 white key to address the amplifier.

   The two LED YAddress digits display the sector-amplifier address entry.

4. The selected amplifier output is placed on the Y Address Bus and is available at the Analog Output panel Yo jack.

2.2.2 X Address (Keyboard)

1. Position the X Address toggle switch to AMP. 2. Depress the black X key.
2. Depress a 0 thru 7 white key to address the sector (computing unit number.)
3. Depress a 0 thru 8 white key to address the amplifier.

   The two LED X Address digits display the sector-amplifier address entry.

4. The selected amplifier output is placed on the Y Address Bus and is available at the Analog Output panel Xo and Xs jacks.

2.2.3 X Address (Digital Computer)

1. Position the X Address toggle switch to TIME.
2. Enter the X address through the digital computer I/O interface.
3. The selected amplifier output is placed on the X Address Bus and is available at the Analog Output panel Xs jack.

2.2.4 Compute Time Period

1. Depress the blue CTP key.
2. Depress a 1 thru 9 white key to select the ten's digit compute time period.

   The unit digit is fixed. The compute time period value can be set only in multiplies of ten.

2.3 Mode Control

Initial Condition...Depress the IC pushbutton to return all system integrators to a slow time, reset state.

Hold...Depress the HD push button to place all system integrators into the slow time hold mode, a state in which ail input summing networks are disconnected from their integrator amplifiers. *Control maybe returned to either the initial condition or operate mode.*

Operate...Depress the OP pushbutton to place all system integrators into a slow time run state.

Repetitive Operation...Depress the RO to speed integrations by 400 times their slow rates, and alternately switch control modes from initial condition to operate, so that the equivalent of a slow time response is compressed, repeated and available for display on an oscilloscope.

2.4 Problem Solution

2.4.1 Graphic Readout... With the X-Y oscilloscope or plotter vertical/horizontal inputs connected to the analog output panel Yo/Xo, for:

Y vs Time...Position the X Address toggle switch to TIME.

Y vs X...Position the X Address toggle switch to AMP.

2.4.2 Scaled Coordinates

Dependent Variables...If [Y/SF] is a scaled variable, *Y the normalized amplifier output/ SF its estimated maximum amplitude,* the + /- Reference is scaled to equal + /- times SF as the full scale graph coordinate.

Time...The full scale coordinates of the Time Base Ramp are zero and the Compute Time Period/B, where B is the program time scale factor.

2.5 Overrange of Amplifier Outputs

2.5.2 Overrange Indicator...When any system amplifier output exceeds approximately +/-10.5 volts, the Control Unit OVLD display will light An LED alarm is also provided on the lower right hand corner of each Computing Unit panel, to light when any of the eight amplifiers are in an overrange condition.

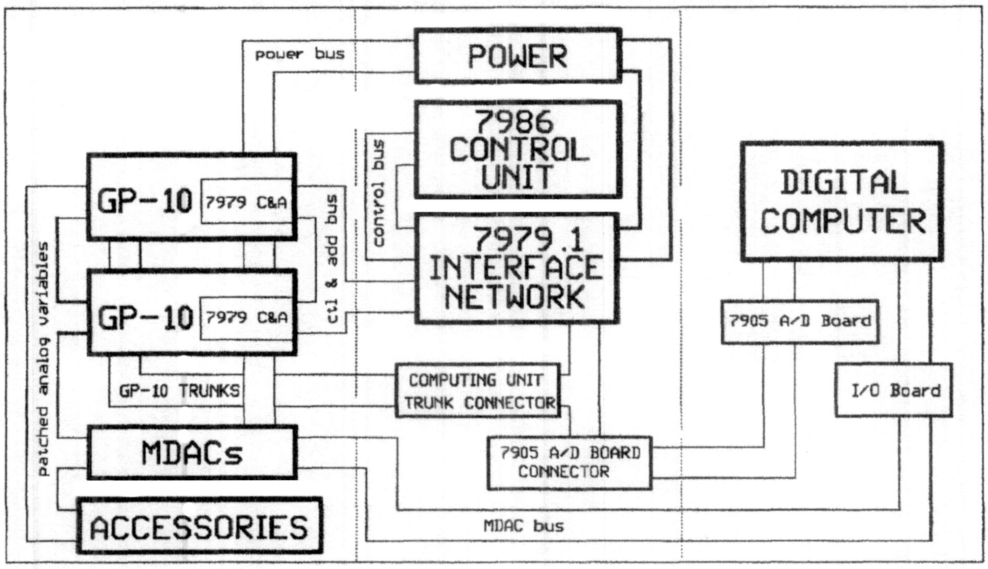
2.5.3 Overrange With Hold...When the OVLD toggle switch is in the W/HD position, an overrange condition will place the system into the Hold mode.

2.6 Power

The AC power toggle switch is located at the Analog Output Panel.

SYSTEM DESCRIPTION

System Organization Schematic, Figure 3-0



A flat cable bus network interconnects operating and control assemblies and provides input/output functions for both analog readout and digital computer interface. Any number of GP-10 computing units may connected to the Central Operations section through the Control & Address Bus. Oscilloscope, recorder or other analog readout instruments may be connected with patch cords at the Primary Chassis front panel or fixed wire cables soldered to the 7979 Interface Network PC board connector. Digital computer address, mode monitor/control and other I/O functions are conducted through the Comdyna 7905 AD/DA Board via the 7905 A/D Board Connector. AD, DA and other interface functions are trunked to GP-10 Computing Units 00 and 01 via the Computing Unit Trunk Connector.

The following are general descriptions of the 7000 system sections.

3.0 CENTRAL OPERATIONS SECTION

3.0 PRIMARY CHASSIS

The distribution and organization of buses originates in the primary chassis.

3.0.1 7979 Interface Network...A PC board assembly that organizes all system readout and control buses, provides decoding, buffering, distribution and I/O connections for analog variables, system control and the digital computer interface.

Analog/Digital Conversion

Internal...The 7979 assembly has a connector for installation and operation of the Comdyna 7093 ADC board.

External...The Primary Chassis may be modified for use with and cable connection to the Comdyna 7905 AD/DA assembly. See para 4.2.

ADC Multiplexer...The X Address bus is the internal ADC input. Under command of the digital computer (see para 2.2.3) the X Address may also serve as the multiplexer for external ADC.

3.0.2 Power Supply...Includes the AC receptacle, fuze, power switch, regulated and unregulated supplies, and precision plus/minus 10 volts reference.

3.0.3 Analog Output Panel-Jacks for convenient patching of output buses, Y *Address, X Address, Time* Base, *Pot (see para 1.0,)* to an oscilloscope, recorder or other analog readout instrument.

3.1 COMPUTING UNITS

3.1.1 GP-10...Traditional analog computers, programmed by patch cord connections.

3.1.2 Accessories... Optional devices, sub-systems, systems used to expand or enhance system operation. Examples are listed as follows:

Multiplying Digital/Analog Converters... Up to sixteen MDAC's per panel enable patch panel digital computer attenuation of analog variables.

7905 Board AD/DA Interface...analog/digital, digital/analog conversion, logic sense and control, time sychronization.

Banana Plug Modules... Patched non-linear and other functions.

709 Variable Diode Function Generator... Straight line approximation of non-linear functions, know adjustments.

705 Variable Diode Function Generator... Straight line approximation of non-linear functions, screw driver adjustments.

771 Transfer Function Simulator.-.Eight common transfer functions for use in control design experiments.

717 Three Mode Controller...Proportional, Rate and Reset control of analog simualtion functions.

809 Analog Signal Processor... Card programmed analog computer.

450 Sine-Cosine Generator...Sine and Cosine Functions for polar/rectangular resolution.

9612 Voltage Controlled Oscillator... Sine wave generator.

9577 Logarithm Generator... Log/anti-log functions.

3.2 CONTROL UNIT

A desk top keyboard and display panel for providing the following operator control and monitor functions.

3.2.1 Integrator Mode Control... Four push buttons enable an operator to place the system integrators simultaneously into the Initial Condition, Hold or Operate modes, *see para 2.3.*

3.2.2 Keyboard..A sixteen position keyboard provides data entry for the following control and monitor functions:

Amplifier Address... Any two computing unit amplifier outputs may be placed on either the Y or X Address buses for readout. Two digit LED displays indicate the selected computing unit and the amplifier output, *see para 2.2.*

Compute Time Period... The two digit display is the Compute Time Period setting, the full scale X axis coordinate as measured in computer time scale seconds, *see para 2.2.4.*

3.2.3 Digital Voltmeter... Voltage measurements of 3 1/2 place accuracy plus sign may be used for setting coefficient attenuators and for static readout of amplifier outputs, see *para 2.1.*

3.2.4 Time Base Ramp...A linear sweep from negative to positive reference, the slope inversely proportional to the Compute Time Period, time scaled for an X-Y recorder when in the slow time, or oscilloscope when high speed repetitive mode.

3.2.5 Overload Indicator... The LED display serves as an alarm when any of the patch panel operational amplifiers exceed approximately +/-**10** volts reference.

Overload With Hold...A toggle switch enables logic to place system integrators into the Hold mode upon an overload condition. An operator can thus determine when any amplifier may have reached a temporary overrange state.

4.0 SYSTEM BUSES

4.1 CONTROL AND ADDRESS BUS

A flat cable that Is common to all computing units; connects the Control and Address assemblies to the Interface Network assembly. Includes the following:

Integrator Mode Control

OP Bus -Initial Condition and Operate control. (IC is low.)

HD Bus -Hold mode control. (Hold when high.)

TS Bus -Control time scale relays. (Slow time is low.)

PS Bus -Manual attenuator setting Mode. (High to set.)

X and Y Address...Two independent channels with identical circuitry; includes select logic and the amplifier output signals.

Computing Unit Enable -1 of 8 code.

Amplifier Selector Logic -Octal 3 bit code.

Analog Bus -Selected amplifier output.

Pot Bus...Input to the digital voltmeter. For setting manual attenuators. Depression of a computing unit, attenuator set-up push button replaces the input with positive 10 volts reference and connects the potentiometer wiper to the bus.

Overload Bus...Pulled low when any computing unit amplifier output exceeds positive or negative reference.

4.2 CONTROL UNIT

The flat cable connection from the desk top, Control Unit to the 7976 board. Includes the following:

Integrator Mode Control...OP, HD, TS and PS buses.

Overload Alarm...Logic "0" when any system amplifier exceeds negative or positive reference.

X and Y Address Selection Codes...Two octal bytes, one select the sector(computing unit,) the other to select the amplifier within the computing unit.

MUX...Logic of the AMP/TIME toggle switch. Controls the multiplexer that enables either the keyboard or microcomputer to select the X Address bus.

Ramp...Analog time base that sweeps from negative to positive reference, the slope inversely proportional to the Compute Time Period.

Xs...Output of the X Address Bus.

Xo...Either Xs or Ramp, as selected by the AMP/TIME toggle switch.

Pot Bus...For measuring and setting coefficient potentiometers.

4.3 7905 AD/DA INTERFACE

Hybrid computing functions connected to the 7905 A/D Board Connector. Provides the following:

Analog/Digital Conversion...Eight multiplixed inputs, one connected to the microcomputer encoded X address, one to the Pot Bus, the remaining six brought out for connection to GP-10 trunk jacks.

Digital/Analog Converstion...Two multiplying and one voltage digital/analog converter inputs/output brought out for connection to GP-10 trunk jacks.

Sense Bits...One sense bits reserved to monitor IC/OP integrator mode logic, two additional available for general use.

Latch State Control Bits...Four latched output bits reserved for control of the system Mode Control IC/OP, Hold, Time Scale and Pot Set Buses.

Analog Compute Time Clock...A internal clock operated by the IC/OP mode logic for use in synchronizing the analog compute time with the AD/DA function generation.

4.4 POWER BUS

Distribution of power to the computing units. Includes:

Precision +10 volts positive reference.

Precision -10 volts negative reference.

Unregulated V+ (regulated to +15 volts at the computing units.)

Unregulated V- (regulated to -15 volts at the computing units.)

Analog, Power and Digital Grounds.

PATCHING

5.0 PATCH PANEL OPERATIONS

Analog Computer Programs

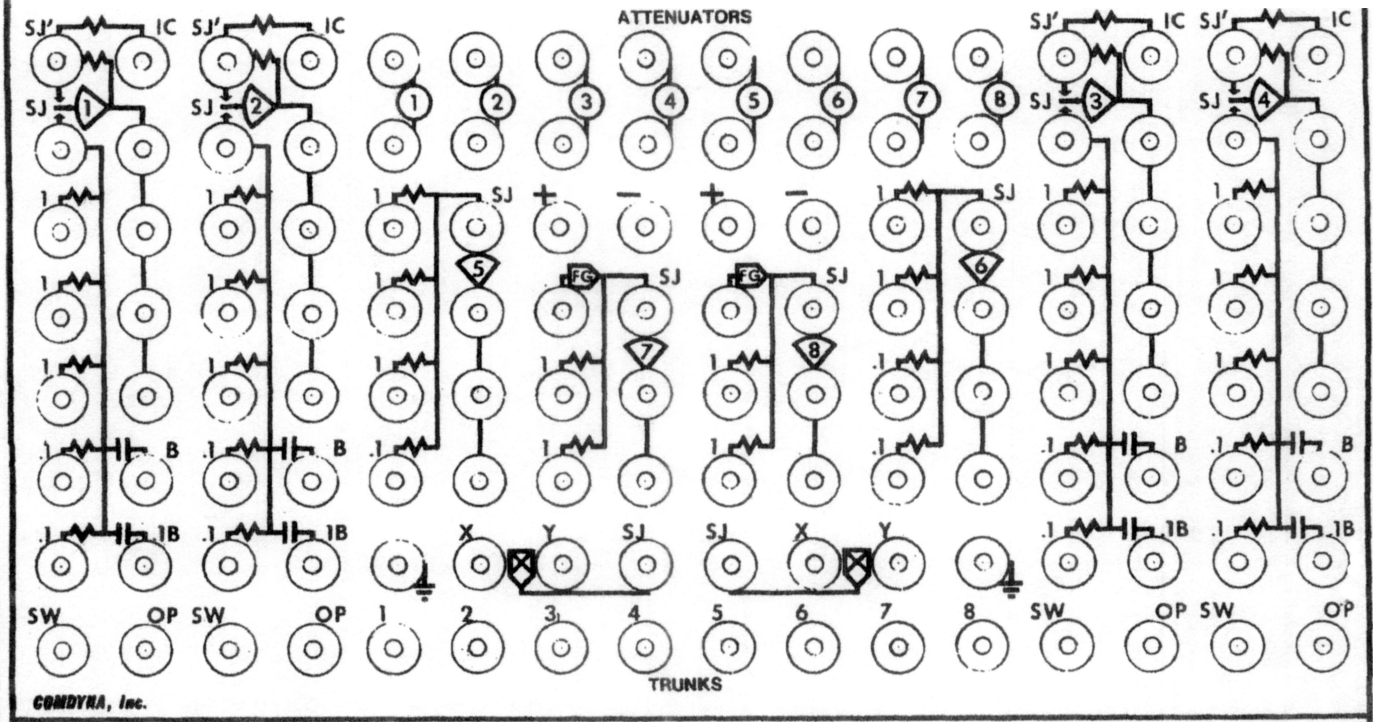
Programs are patched at the GP-10 computing unit and accessory panels.

Interconnections.

Interconnections to/from the GP-10 panels may be made directly with patch cords or indirectly through TRUNK patch panel jacks. Eight patch panel TRUNK and four FG (function generator) lines are terminated in the computing unit trunk connectors, as listed below:

1. Amp 7 **FG** input.
2. Amp 7 **SJ.**
3. Amp 8 **SJ.**
4. Amp 8 **FG** input.
5. TRUNK 1.
6. TRUNK 2.
7. TRUNK 3
8. TRUNK 4.
9. TRUNK 5.
10. TRUNK 6.
11. TRUNK 7.
12. TRUNK 8.

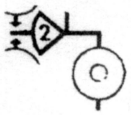
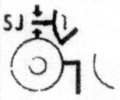
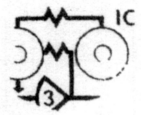
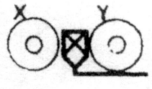
GP-10 ANALOG COMPUTING UNIT



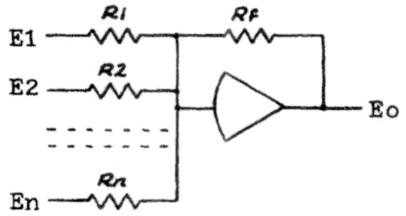
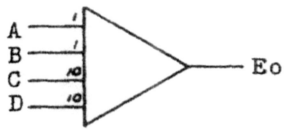
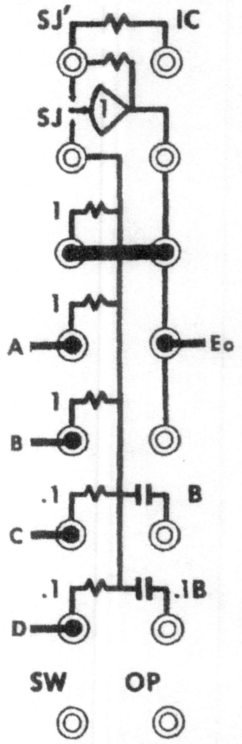
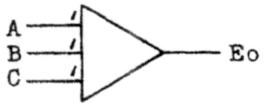
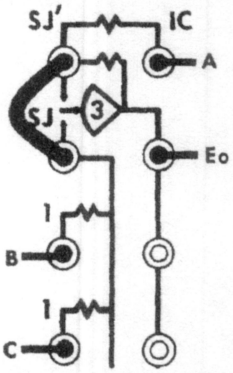
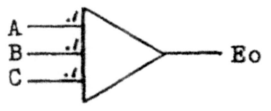
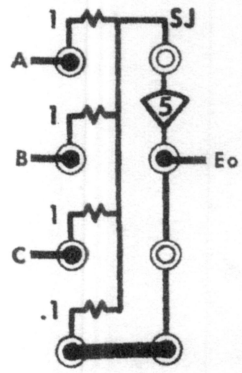
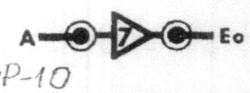
Patch panel graphics represent networks as they are applied in normal analog computer programming. All amplifiers may be used as summers or high gain operational amplifiers; amplifiers 1 thru 4 have electronic switch networks and may be programmed as integrators, track/store amplifiers and single pole, double throw electronic switches. Initial Condition Attenuator wipers are connected to the "IC" inputs for entering manually set constants. Eight Attenuators have their inputs and wipers terminated at the patch panel. Multiplier networks have current outputs; with one amplifier each may be used as a multiplier, divider, squarer or square root extractor. Eight trunk jacks may be used to route external inputs and outputs. The two "FG" trunks that are connected to amplifiers 7 and 8 are reserved for diode function generator inputs.

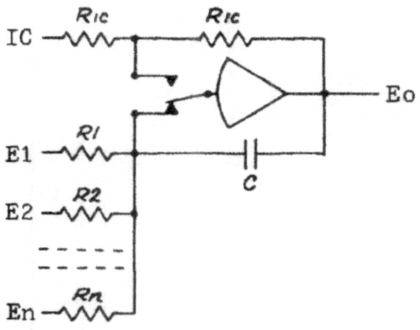
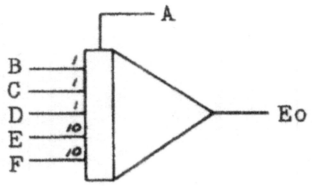
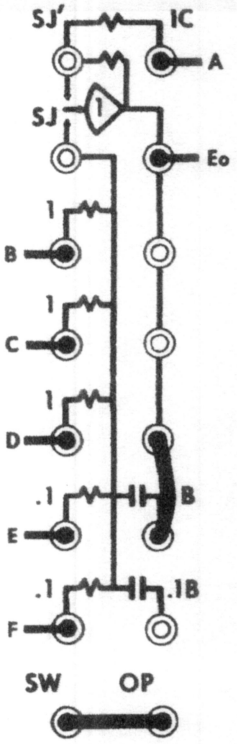
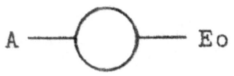
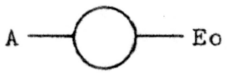
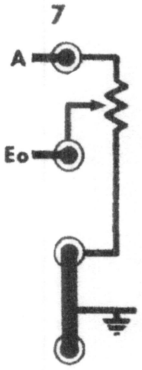
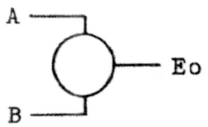
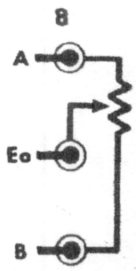
The following is a description of patch panel symbols:

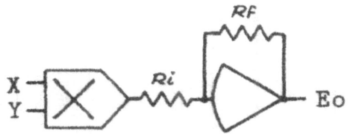
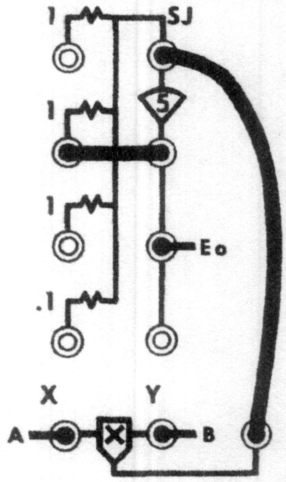
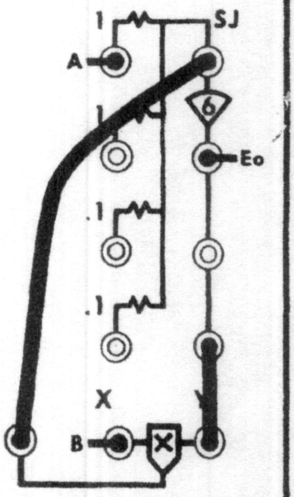
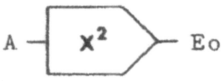
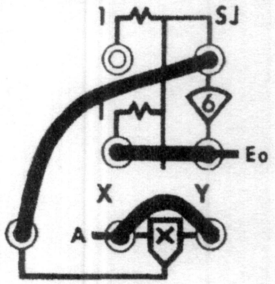
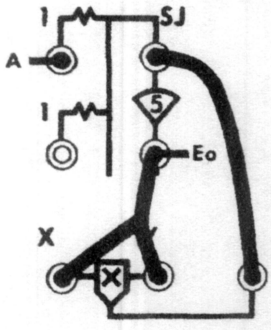
SYMBOL	COLOR CODE	DESCRIPTION
+	Orange	Positive reference, considered unity, 1.000, for formalized programming. (Actual value is 10 volts.)
−	Yellow	Negative reference.
⏚	Black	Analog Signal Ground.
6	Yellow	Manual attenuator input.
6	Yellow	Manual attenuator wiper or output.
4 TRUNKS	White	Trunk lines. Routing determined by user.

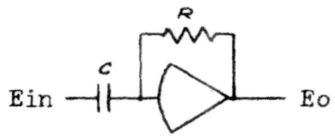
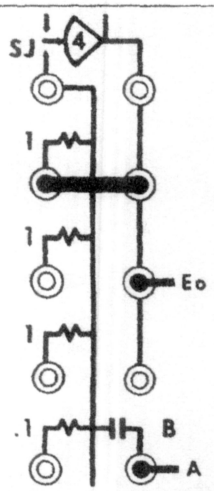
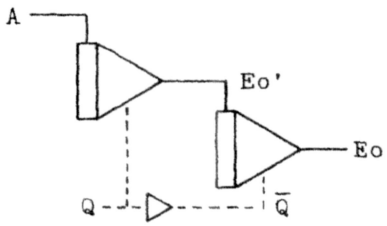
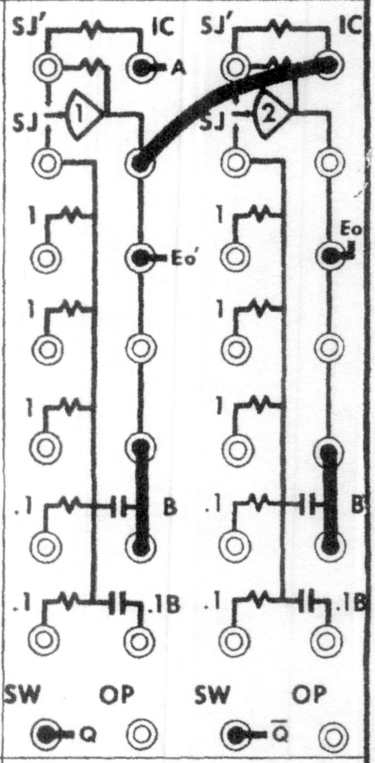
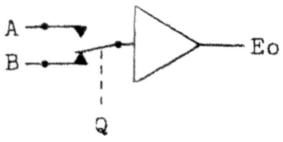
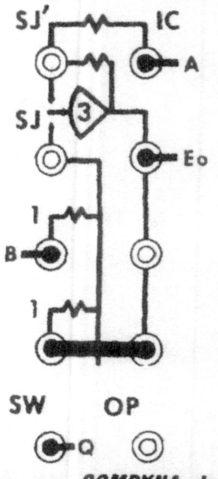
SYMBOL	COLOR CODE	DESCRIPTION
		High gain operational amplifier.
		High gain operational amplifier with electronic switch.
	Red	Amplifier output.
	Gray	Summing junction. (Active for amplifiers 1 thru 4 when a logic "1" is applied to the "SW" switch control jack or when there is no switch control patching.)
	Gray	Alternate summing junction for amplifiers 1 thru 4. (Active when a logic "0" is applied to "SW.")
	Green	Standard input summing resistor, normalized. (Actual value is 50K ohms.)
	Green	Summing resistor that has a value one tenth the standard. (Actual value is 5K ohms.)
	Blue	Standard integrating capacitor input, normalized. (Actual value is 20 ufd in the slow time mode and .05 ufd in the repetitive operation mode.)
	Blue	Integrating capacitor that has a value equal to one tenth the standard. (Actual value is 2 ufd in the slow time mode and .005 ufd in the rep. op. mode.)
	Green	Resistor network. Amplifier becomes an inverter when SJ' is active. When SJ is active, amplifier may be a summer by patching SJ and SJ' together. "IC" jack is the normal integrator initial condition input as it is connected to the associated Initial Condition Attenuator wiper. (Value of resistors is 50K ohms.)
	White	Electronic switch control input. With a logic "0" (ground or positive voltage) the SJ' summing junction is active and SJ shuts off. With a logic "1" (-5 thru -15 volts) SJ is active and SJ' shuts off. With "HD" logic (-2 thru -3 volts) SJ' shuts off, the SJ summing junction is active but the summing resistor network is disconnected.
	White	The system's operate bus; provides integrator mode control logic as selected by the operator.
	Brown	Multiplier network. "X" and "Y" are inputs.
	Gray	Multiplier output, a current that is proportional to the product of inputs "X" and "Y."
	Brown	Trunks allocated as function generator inputs to amplifiers 7 and 8.

PATCH PANEL OPERATIONS

FUNCTION	OPERATION	PATCHING
Summer (amplifiers 1-4)	Fundamental Summer Operation  Eo = -Rf(E1/R1 + E2/R2 ... + En/Rn)  Eo = -(A + B + I0C + 10D) NO PATCHING TO SWITCH CONTROL "SW"	
Summer (amplifiers 1-4 with IC networks)	 Eo = -(A + B + C) NO PATCHING TO SWITCH CONTROL "SW"	
Summer (amplifiers 5 & 6) yes has 2 "1" inputs 2 ".1" inputs	 Eo = -(.1A + .IB + .IC)	
Inverter (amplifiers 7 & 8) more possibilities than for GP-10	Eo = -A This is for GP-6, not GP-10	

FUNCTION	OPERATION	PATCHING
Integrator (amplifiers 1-4)	Fundamental Integrator Operation  $Eo = -1/C\int(E1/R1 + E2/R2 \ldots + En/Rn)dt - IC$  $Eo = -\int(B + C + D + 10E + 10F)dt - A$	
Attenuator (pots 1 - 6) 8	 Eo = K(A)	
Attenuator (pots 7 & 8)	 Eo = K(A)	
Voltage Divider (pots 7 & 8)	 Eo = K(A - B) + B	

FUNCTION	OPERATION	PATCHING
Multiplier	Fundamental Multiplier Operation  Eo = -(X*Y)  Eo = -(A*B)	
Divider	 Eo = -(A/B) A > 0	
Squarer	 Eo = -A²	
Square Root	 Eo = -√A A < 0	

FUNCTION	OPERATION	PATCHING
Differentiator (amplifiers 1-4)	Fundamental Differentiator Operation  Eo = -RC*dEin/dt  Eo = -dA/dt NO SWITCH CONTROL PATCHING	
Track/Store (amplifiers 1-4)	 Eo' = -A when Q is a logic 0 Eo' = -A' when Q is a logic 1 A' is the stored value of A when Q switches from 0 to 1 Eo = A'(n-1) A'(n-1) is the previous value of A'	
SPDT Electronic Switch (amplifiers 1-4)	 Eo = -A when Q is a Logic "0" Eo = -B when Q is a Logic "1"	

SCHEMATICS AND CIRCUIT DIAGRAMS

7000 PRIMARY CHASSIS

The Primary Chassis is the central power and operating system for all 7000 computing functions.

Power...The main power supply and 7913 Regulator Board produces an unregulated +/-18 volts for distribution to and regulation by the individual computing units. The 7913 board also produces a regulated +/-15 volts for use by the 7976 Interface Board, the system regulated 5 volts Vcc, and the system +/-10 volts precision reference.

Bus Distribution...There is a power bus and network of flat cable buses.

Power Bus. All power and ground connections are made at the Barrier Strip.

Flat Cable Buses. All flat cable buses (Control and Address; Control Unit; Micropatch; Digital Computer I/O) are connected to and distributed by the 7976 Interface Board.

Readout...The Analog Output Panel provides the following:

Yo ...Selected Y axis output.

Xo...Selected X axis output.

Xs...Output of the X Address multiplexer.

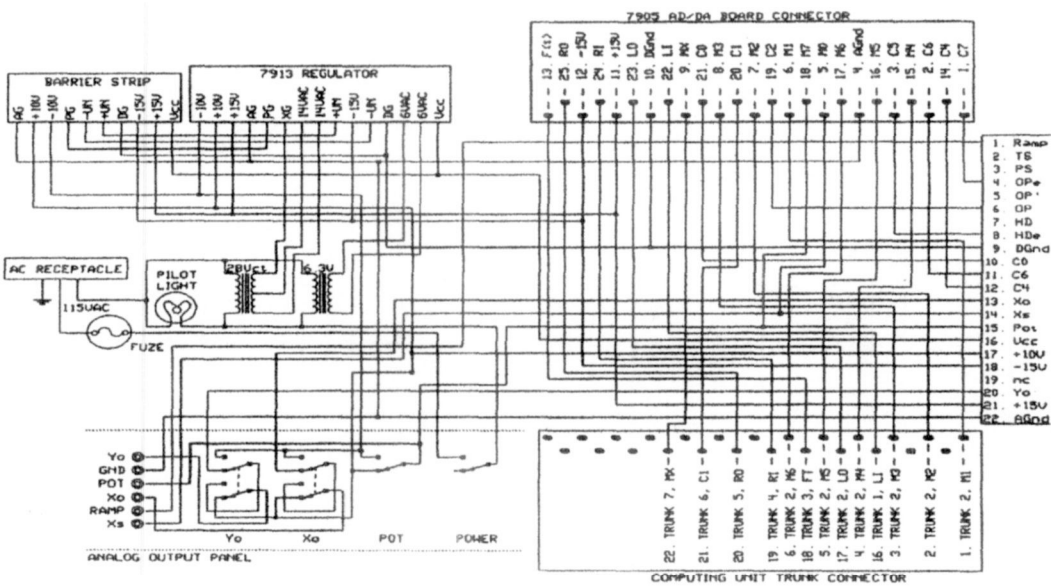
RAMP...X axis time base.

POT...Pot Set Bus, input to the digital voltmeter.

GND...Signal Ground.

Slave Connections...Systems may share a common control by common connections to the 7976 Interface Network connector lugs: TS-time scale bus; PS-pot setting mode bus; OP-IC/OP mode control bus; HD-hold mode bus. All are open collector, TTL logic control buses.

Schematic



INSTALLATION

A 7000 system is typically furnished as rack mountable units. Unless otherwise indicated by special instructions, units are to be mounted in a standard rack or enclosure, stacked in a vertical column with the Primary Chassis at the bottom and computing units in ascending orders of their address locations (address 00 the lowest.) if rack mounted accessories are to be placed between computing units, their locations shall be indicated by special instructions, or marker tabs indicating the ascending order of all units.

The Power Bus cable is furnished connected to the Barrier Strip. PowerBus connectors are to be plugged into the 7979 Control and Address boards of individual computing units. Accessories requiring power will likely be furnished with a wiring harness, labeled for connection to Barrier Strip posts.

The Control and Address Bus cable will likely be shipped connected to the 7976 Interface Network board. Remaining connectors are to be plug to the computing units' Control and Address Bus tabs.

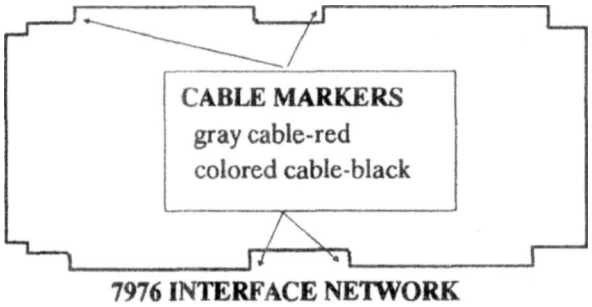
Setting the Control Unit on a desk surface outside the Primary Chassis, the Control Unit Bus cable is then fed under the Primary Chassis and plugged to the 7976 Interface Network board Control Unit tab.

Where 796C MDAC units are furnished, the flat cable is connected from the 7979 Interface Board MICROPATCH connector tab to the 796 MDAC board tabs. The 796C chassis is shipped with a power harness to be connected to the Barrier Strip.

The power receptacle is included with the Primary Chassis. For 230VAC operation, the system shall be equipped with a step down transformer before the standard 115 power supply.

Interface (Readout, Mode Control, etc.) connections may be made at 7979 Interface Network board connector eyelets. (See page A1.)

FLAT CABLE CONNECTOR ALIGNMENT



7976 INTERFACE NETWORK

EQUIPMENT CONFIGURATION

PRIMARY CHASSIS:

POWER SUPPLY	7905 ADC	SPECIAL FEATURES
7117	NO	NONE

COMPUTING UNITS

LOC	DESCRIPTION	CAP.	MULT.	SPECIAL FEATURES
00	GP-10	std	983/. 1	none
01	GP-10	std	983/. 1	none
02	GP-10	std	983/. 1	none
03	GP-10	std	983/. 1	none
04	GP-10	std	983/. 1	none
05	GP-10	std	983/. 1	none
06	GP-10	std	983/. 1	none
07	GP-10	std	983/. 1	none

ACCESSORIES

771 Transfer Function Simulator/717 Transfer Function Simulator

709 Variable Diode Function Generator

7913.1 REGULATOR

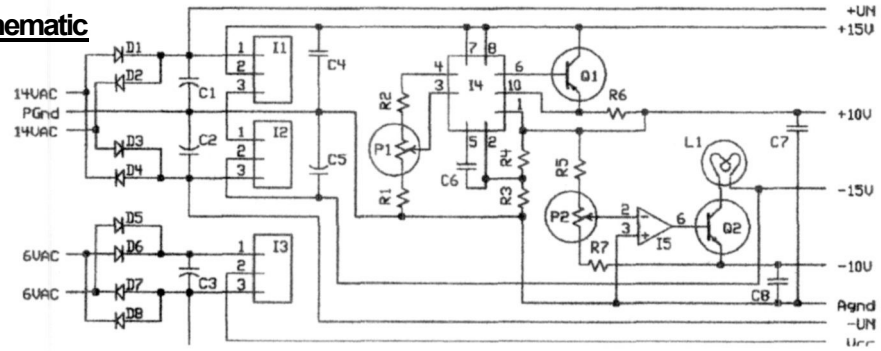
The 7913 assembly rectifies/filters from the 28 VCT secondary to produce an unregulated +UN and -UN outputs, which are also regulated as plus/minus 15 volts, precision plus/minus 10 volts reference and Vcc (plus 5 volts.)

Positive reference is produced by ua723 regulator 14. Negative reference is inverted positive reference. Lamp L1 offers negative reference output protection.

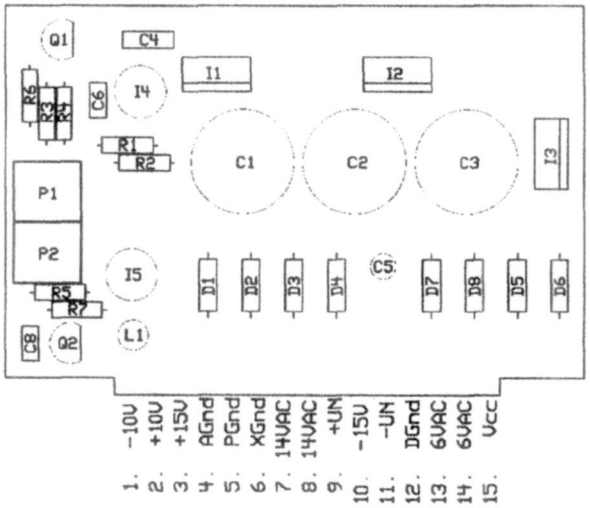
Reference Adjustments

1. Adjust potentiometer P1 until the positive reference equals +10.000 volts.
2. Adjust potentiometer P2 until negative reference equals the inverted positive reference.

Schematic



Assembly Drawing



Parts list

R6	10	ohm	
R2	2.32	K#*	
R3	2.43	K#	
R5,R7	4.99	K#	
R1	6.04	K#	
R4	9.76	K#	
L1	12V .04A	INC	
P1,P2	50	ohm	
C1,C2,C3	2200	ufd	elec
C4	.1	ufd	cer
C5	1	ufd	tant
C6	100	pfd	cer
C 8	.01	ufd	cer
D1 - D8	1N4001		
Q1	2N4124		
Q2	2N4403		
11	ua7815		
12	ua7915		
13	ua7805		
14	ua723		
15	Mc1741CG		

NOTES: #metal film resistor

*value may be altered

Rectifier diodes D1 - D4 may be 2N5401 for high current applications.

INTERFACE NETWORK, 7976

The 7976 Interface Network board is a central distribution for the following 7000 system busses.

1. Digital Computer
2. Control Unit
3. Micropatch
4. Control and Address
5. Analog/digital Converter Connector
6. Primary Chassis Connector

1. Digital Computer

The Digital Computer bus is organized for direct connections to the INS8255N programmable peripheral interface device. The three parallel 8 bit bytes are used in either a data input or data output mode. A mode change alters only the Port B byte which is allocated for data transmission only. The following is a distribution of the three I/O bytes.

Port B — Latched output for data output mode.

Data B0-B7

1. Data is buffered and level changed to +15,0 volts by hex buffers I3 & I4 for distribution by the Micropatch bus.
2. Data is available to the ADC converter for setting the internal DAC.
3. With a modification, bits B0-B3 may be outputs to the Control Unit bus.

Unlatched input for data input mode.

1. Data may be read from the ADC Connector.
2. When tri-state gates I2 are enabled, B0-B3 may be read from the Control Unit bus.

Port A — Latched output.

Address A0-A7

1. A0-A2, A4-A6, A7 are buffered and level changed by I4 & I5 for distribution by the Micropatch bus. A0-A2 are the component select bits. A4-A6 are decoded by I6 to be the one of eight, M(0)-M(7), unit enable.
2. A0-A2 and A4-A6 are also inputs to multiplexers I8 and I7. The outputs of I8 & I7 are the X Address select logic.

Port C — Latched output.

Instruction C4-C7

C5-C7 are decoded by I1 to produce eight instruction bits. A C4 low enables the decoder. The eight bits are distributed as follows:

1. 00, 02 & 07 are buffered and level changed by I5 for distribution by the Micropatch bus.
2. 07 is also the I2 tri-state gate enable.
3. 03-06 are terminated at the ADC Connector.
4. 01 is connected to the Control Unit bus.

Port C	Unlatched input.
Sense C0-C3	1. CO is received from the Control Unit bus. 2. C1 is unused. 3. C2 is connected to the OP mode control bus. 4. C3 is connected to the ADC Connector.

2. Control Unit

The Control Unit bus contains terminations for the 7986 Control Unit.

Digital Computer Interface...Keyboard data is transmitted to the digital computer via bits B0-B3. Instruction bit 01 (Ask) is the digital computer ready command. CO is data ready logic.

Amplifier Address...Address bits X0-X2, X4-X6, Y0-Y2 & Y4-Y6 are outputs of Control Unit latches. X0-X2 and A0-A2 are multiplexed by I8 to become the X address amplifier select logic. X4-X6 and A4-A6 are multiplexed by I7 to become the computing unit enable. Control bit MX (determined by the X Address toggle switch position) controls both the I7 & I8 multiplexers. When MX is high the Control Unit outputs are enabled.

Multiplexer outputs X0-X2 and Control Unit outputs Y0-Y2 are buffered by I11 for distribution by the Control and Address bus. Multiplexer outputs X4-X6 are decoded by I9 to be the X address computing unit enable, X(0)-X(7). Y4-Y6 are decoded by I10 to be the Y address computing unit enable, Y(0)-Y(7).

Overrange Indicator...The OVLD bus is buffered by a buffer of I12 for transmission to the Control Unit. A low state indicates an overrange condition.

Mode Control...Mode control originates at the Control Unit. HD', OP', PS' & TS' are buffered by buffers of I12 and distributed by the Control and Address bus and the Primary Chassis connector. OP' is sensed by C2 for digital computer monitor of the analog mode control.

Analog I/O...The time base sweep (Ramp) originates at the Control Unit and is transmitted to the Primary Chassis connector. The X address output (Xs) is transmitted to the Control Unit for input to the digital voltmeter and selection by the X Address toggle switch. The X Address toggle wiper (Xo) is transmitted to the Primary Chassis connector for output.

The Pot bus is a common analog input to the digital voltmeter. It carries attenuator setting voltages from the computing units, however, a Primary Chassis connector input is available for general external voltage measurements.

3. Micropatch

The Micropatch bus contains logic to select either the Micropatch Attenuator-Switch or Multiplying Digital/Analog Converter networks and to enter data into these units. All logic is buffered and level changed by the gates of I3, I4 & It to be +15,0 volts.

Unit Select...A0'-A2' is the unit select logic that is common to all networks.

Network Enable...A4'-A6' are decoded by I6 to produce the network enable bits M(0)-M(7).

Data...B0'-B7' are the data byte for entering Micropatch programming words or MDAC settings.

Commands Clear...Instruction bit 00.
Pulse...Instruction bit 02 (sets data latches.)

Instruction bit 07 and address bit A7 are provided with no defined purpose.

4. Control and Address

The Control and Address bus contains mode control logic, address logic and analog signals for connection to computing unit 7979 Control and Address boards.

X Address...X0-X2 is the amplifier select logic that is common to all X multiplexers. X4-X6 is decoder by I9 to produce multiplexer enable bits X(0)-X(7).

Y Address...Y0-Y2 is the amplifier select logic that is common to all Y multiplexers. Y4-Y6 is decoded by I10 to produce multiplexer enable bits Y(0)-Y(7).

Mode Control...TS, PS, HD and OP are the buffered logic controls for the system's time scale, pot set, hold and operate modes.

Overrange...An overrange condition pulls the common OVLD bus low. The OVLD bus is buffered by a buffer of I12 and transmitted to the Control Unit.

Analog X Address Output...Xad is the common output for the X multiplexers. Xad is buffered by follower amplifier A to become Xs.

Y Address Output...Yad is the common output for the Y multiplexers. Yad is buffered by follower amplifier B to become Yo.

Attenuator Setting Measurement... Pot is the bus that is used to transmit computing unit attenuator setting voltages to the Control Unit digital voltmeter.

Internal Digital/Analog Converter...DAC is the bus that carries the output of the internal digital/analog converter that is furnished with the analog/digital converter assembly.

5. Analog/Digital Converter Connector

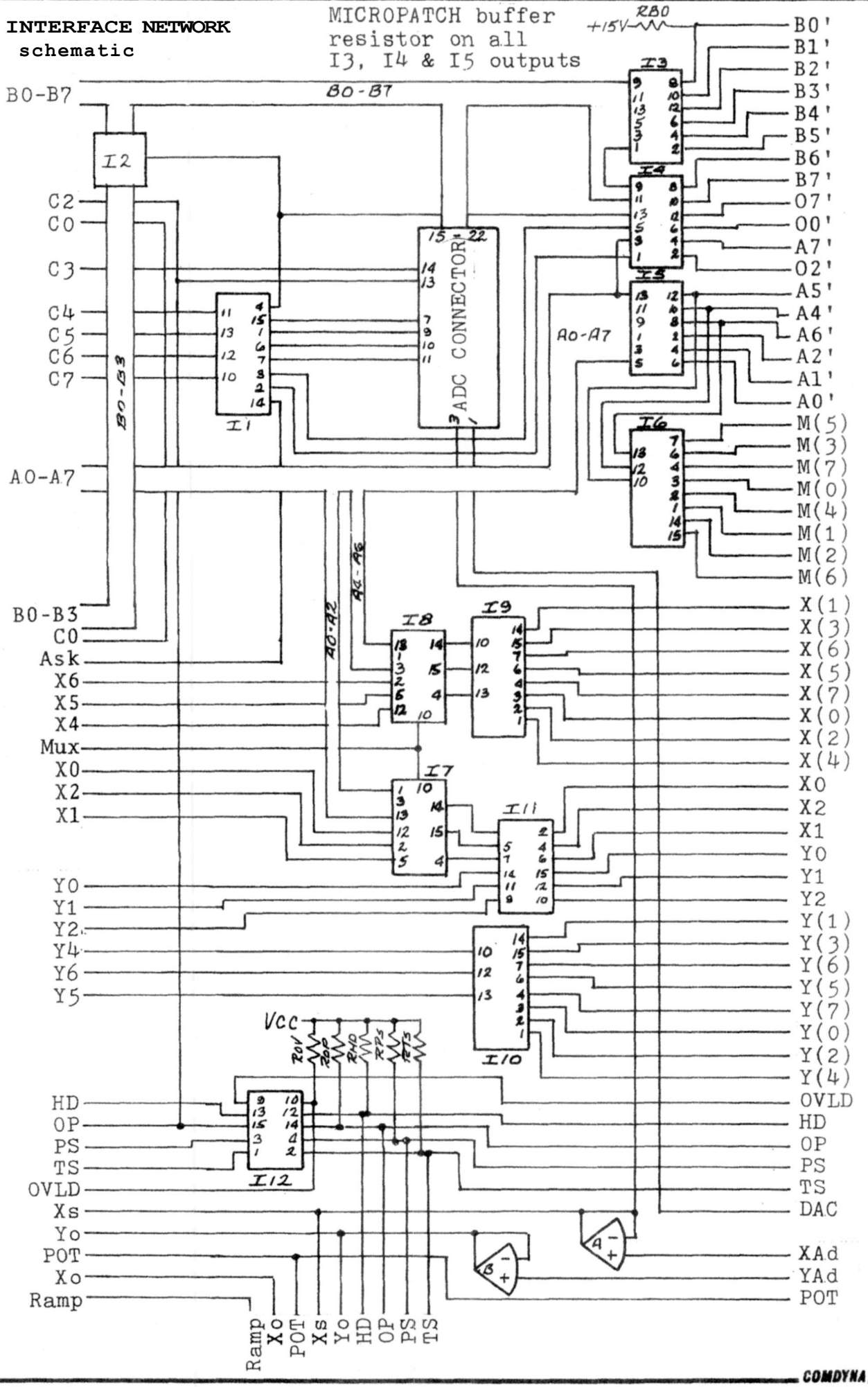
The ADC connector provides power, controls and a data link for operation of the plug-in analog/digital converter board assembly.

Analog Input...Xs (X Address Output)

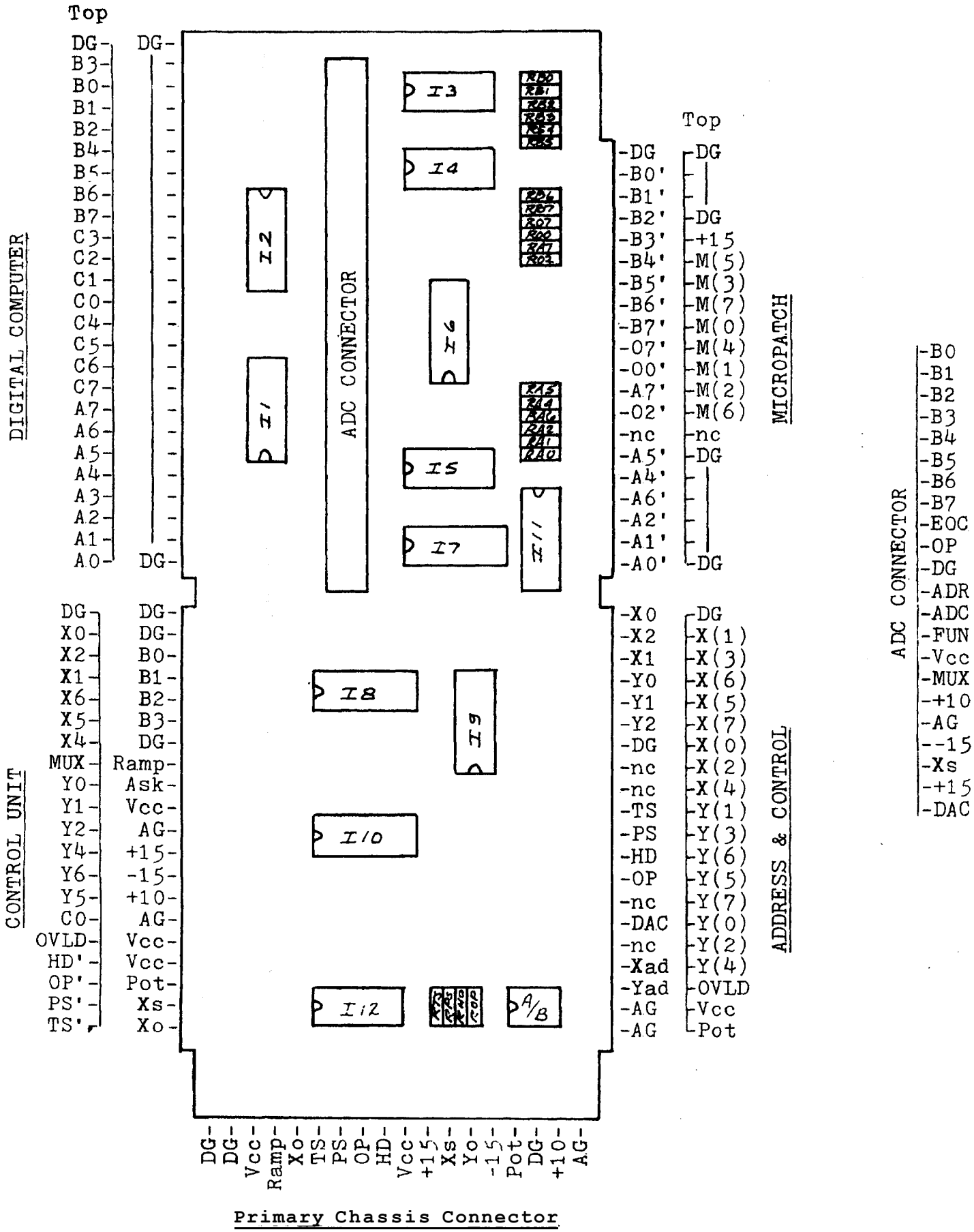
Controls ADC...Instruction bit 05 starts the converter process.

FUN...Instruction bit 04 gates the ADC start and the DAC set with internal clock pulses.

7976 **INTERFACE NETWORK**
schematic



7976 **INTERFACE NETWORK**
assembly drawing



A10

ADR...Instruction bit 06 enables the high resolution data bits onto the Port B bus.

MUX...Instruction bit 03 enables the low resolution data and the sign bit onto the Port B bus.

Clock Reset...The OP' mode control logic resets the clock pulse integrator.

Sense...Port C bit C3 senses the end of conversion (EOC) logic.

Data...Data is transmitted from the ADC and to the DAC via bits B0-B7.

DAC...Output of the internal digital/analog converter.

6. Primary Chassis Connector

The Primary Chassis connector contains power inputs, mode control and analog busses for system input/output connections.

Power Inputs are +/-15 volts, +/-10 volts reference and Vcc (+5 volts.) All Control Unit power is transported via the Control Unit bus. Vcc is made available to the computing units via the Control and Address bus.

Mode Control...Buffered TS, PS, HD and OP are available for external connections.

Analog Xo and Yo are the primary outputs for use as the horizontal and vertical Inputs to an oscilloscope display or XY recorder.

Xs is available for use as a second vertical input channel, digital computer addressed variable or other purpose.

Ramp is available for use as a time base sweep.

The Pot bus is connected for use as an external input to the Control Unit digital voltmeter.

Parts List

I1,I6,I9,I10	...	4028BCN		
I3,I4,I5,I12	...	7417N		
I2	...	74LS126N		
I7,I8	...	4053BCN		
I11	...	4050BCN	Micropatch buffer resistors...	15K
Amps A/B	...	MC1458N	Mode buffer resistors ...	4.7K

A11

CONTROL UNIT, 7986

The 7986 Control Unit provides the following operating function:

1. Integrator mode control.
2. Slow and fast time base ramps.
3. X and Y address codes.
4. Digital voltmeter readout.
5. Amplifier output overrange indication.
6. Keyboard communication with an external digital computer.

1. Integrator Mode Control

The four mode control push buttons with interlocking diode network (D1-D10,) quad S-R latch I3 and gates A-D produce logic control bits PS, TS, OP and HD. LED indicators L12-L15 show the mode state.

Mode States

IC...Initial Condition Mode, slow time scale. Logic to reset computing unit integrators.

HD...Hold Mode, slow time scale. Logic to disconnect input summing resistor networks from integrator summing junctions.

OP...Run Mode, slow time scale. Logic to manually switch integrator modes from a hold or reset to a run state.

RO...Repetitive Operation, fast time scale. Logic to de-energize computing unit time scale relays and alternately switch integrator modes from reset to run states.

Control Logic... Control logic from the four mode states is the following four buses

PS Bus...High in the initial condition mode. Used for attenuator setting. Closes integrator hold mode switches to prevent a setting error from a floating summing resistor network.

HD Bus...High for the hold mode. High logic opens integrator hold mode switches.

OP Bus...Low for the initial condition mode; high for the hold and run modes. Alternates between high and low for repetitive control.

TS Bus...High for the initial condition, hold and run modes; low for repetitive operation. Logic controls the integrator time scale relays and time scales the time base ramp.

2. Slow and Fast Time Base Ramps

A linear time base ramp (used to generate time response curves and plots) is produced by the 980 Timer Circuit that plugs into the 980 Timer Connector. The ramp sweeps from negative to positive reference. It's slope is proportional to the reciprocal on the compute time period (see below.) Initial condition and run modes are controlled by the OP bus that is shown as connector control input OPI. OPO is produced by the timer circuit and is gated to be the OP bus logic during repetitive operation.

Compute Time Setting

Depressing the blue key (CTP) initiates the computing time setting. The Key Data Bus is decoded by I15 to set a flip-flop of I16 that enables latch I10 to set to the next key depression. The latch output (bits D0-D3) drive LED L2 which is the ten's digit of the compute time period display. LED L1 permanently displays "0." Bits D0-D3 also control the slope of the time base ramp so that either a fast or slow time base exactly sweeps between negative and positive reference during the compute time period.

3. Y and X Address Codes

The Key Data Bus with depression of the red (Y) push button is decoded by I15 to set a flip-flop of I17 to enable latch I14 to set to the next key depression. The output of I14 is octal code Y4, Y5, Y6 which, through decoder driver I9, drives LED L6 and is the computing unit selector for the Y Address Amplifier Output. A set of I14 shifts the enable to I13 to set to the next key depression. The output of I13 is octal code Y0, Y1, Y2 which, through I8, drives LED L5 and is the amplifier selector for the Y Address Amplifier Output.

Depression of the black (X) push button performs an identical operation with quad flip-flop I16, latches I12-I11, decoder drivers I7-I6, LED's L4-L3. I12 produces the X Address computing unit selector as octal code X4, X5, X6; I13 produces the amplifier selector as octal code X0, X1, X2.

X Address Toggle Switch

The X Address Toggle Switch is a double pole, double throw switch. One pole switches the time base ramp or the X Address Amplifier Output as the Xo readout terminal, The second pole provides logic bit MX that controls the X address multiplexer located within the 7979 Interface circuit. At the "TIME" position, MX is low and the X address code is provided by the external digital computer. At the "AMP" position, MX is high and the code is provided by the keyboard as described above.

4. Digital Voltmeter Readout

The digital voltmeter, integrated circuit I4 plus associated circuitry, is displayed by LED's L7 thru L10. Potentiometer P1 is the full scale adjustment that should be set so that a 1.000 reading appears with a +Ref (10 volts) input. A polarity indicator "-" shows if the input is negative. Analog inputs are selected by the DVM Toggle switch. One pole is connected to the X Address Amplifier Output while the second pole is connected to the POT bus. A technical description of the DMV circuitry may be obtained from Intersil data sheet 12-77-00B.

5. Amplifier Output Overrange Indication

An amplifier overrange condition is displayed by LED L11. When the OV bus is pulled low (indicating that at least one system amplifier is exceeding its maximum amplitude range) transistor Q3 holds LED L11 on.

Overrange With Hold

The OVLD w/Hold Toggle switch connects the collector of Q3 to a hold mode latch input of I3. An OV low condition thus sets the integrator mode control into a hold state. Latch reset occurs with a normal push button mode control entry.

6. Keyboard Communication with an External Digital Computer

Keyboard entries may be transmitted as hexadecimal data bytes via the 7979 Interface circuit. With an ASK high pulse, a flip-flop of I17 is cleared and output CO is set low. Any keyboard entry will set CO high. Keyboard data is transmitted as bits B0-B3.

Parts List

R13	33	ohm	L1-9,11-15	MAN 72A
R14-18	180	ohm	L10	MAN 73A
RA-RG (led's)	300	ohm		
R19,21	4.7	K	D1-D10	1N4148
R2,3	10	K		
R8,9,11,12,20,22-24	15	K	Q1,2,4,5	2N4124
R4	49.9	K	Q3	MPA A13
R1,5,10,25	100	K		
R6	162	K	I1	74LS05
R7	1	M	I2	79MGU
			I3	74279
P1	10	K	I4	ICL 7107
			I5-9	7447
C1	100	pf	I10-14	74C173
C5	.01	uf	I15	4028
C3	.047	uf	I16,17	74C175
C2,C8	.1	uf	I18	74C922
C4	.22	uf	(A,B,C,D)	74LS03
C6,C7	1.0	uf		
			S1	DPDT toggle
			S2,S3	SPDT toggle
			data switches	Oak Series 399

TIMER, 980

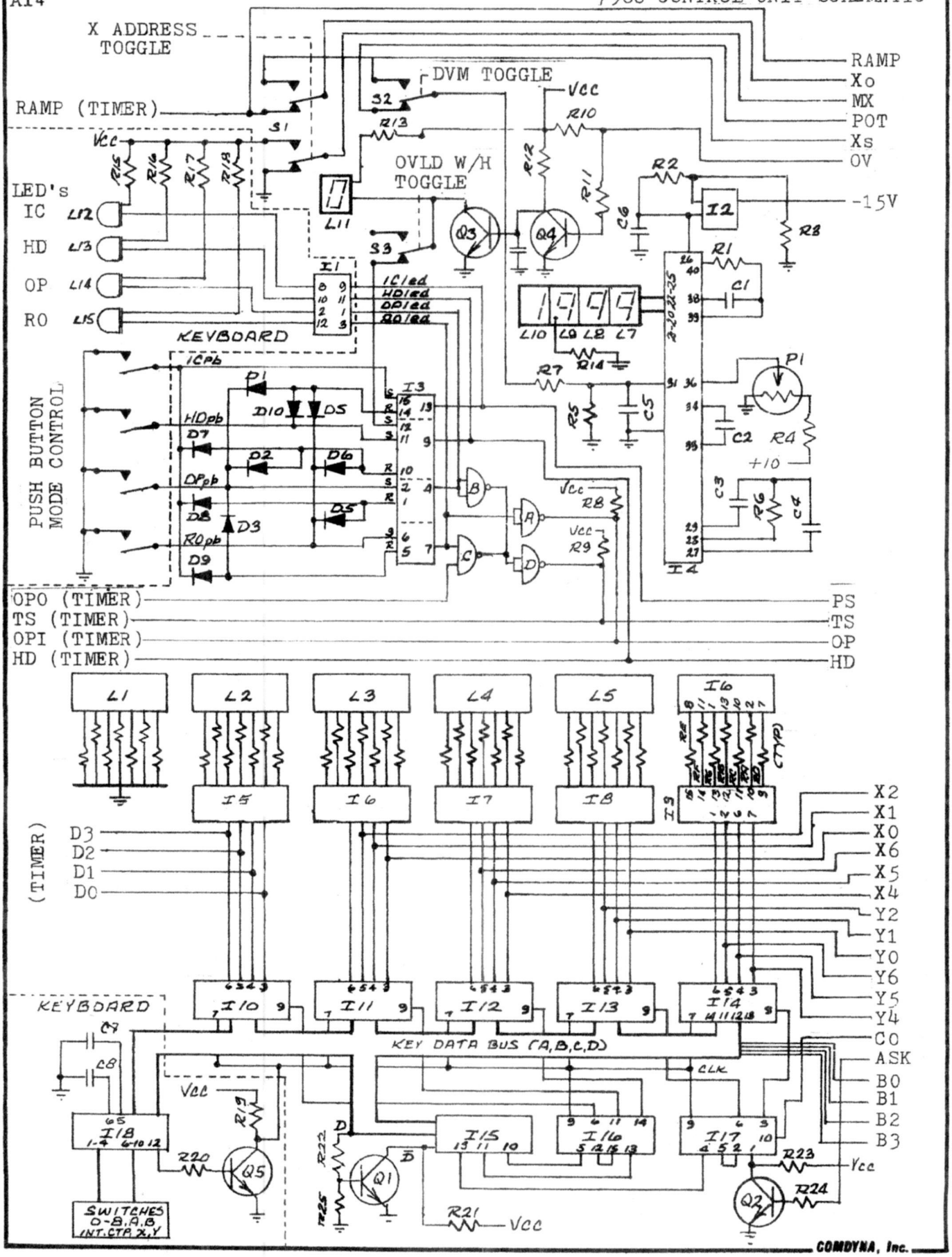
The 980 circuit board plugs into the 980 Timer Connector located within the 7986 Control Unit assembly. It produces slow and high speed linear ramps for use as the horizontal time base inputs to XY recorders and display oscilloscopes. The ramp output is from integrator amplifier C which receives a negative reference initial condition from +10 volts through resistors R28 and R29 and FET Q10. The time base gains are digitally set through I1 which is a multiplying digital/analog converter configured with amplifier A to produce a reciprocal of the four bit setting (D0-D3.) The output of A is inverted by amplifier B and then directed to the time base integrator through FETS Q6,Q7,Q8. Q7 conducts during slow time and repetitive operation; Q6 conducts only during repetitive operation. Both Q6 and Q7 are shut off with hold mode logic Hd. Q6 is also controlled by time scale logic TS. OPI is the system's mode control bus. OPO is the repetitive mode control logic produced by comparator amplifier D and monostable transistors Q12 and Q11.

Adjustments

PI adjusts the slow time ramp slope; P2 adjusts the high speed ramp slope. Both are adjusted to match system integrator time constants. The time base ramp slopes are adjusted to equal the same time base ramp slopes that are programmed and run on a computing unit.

A14

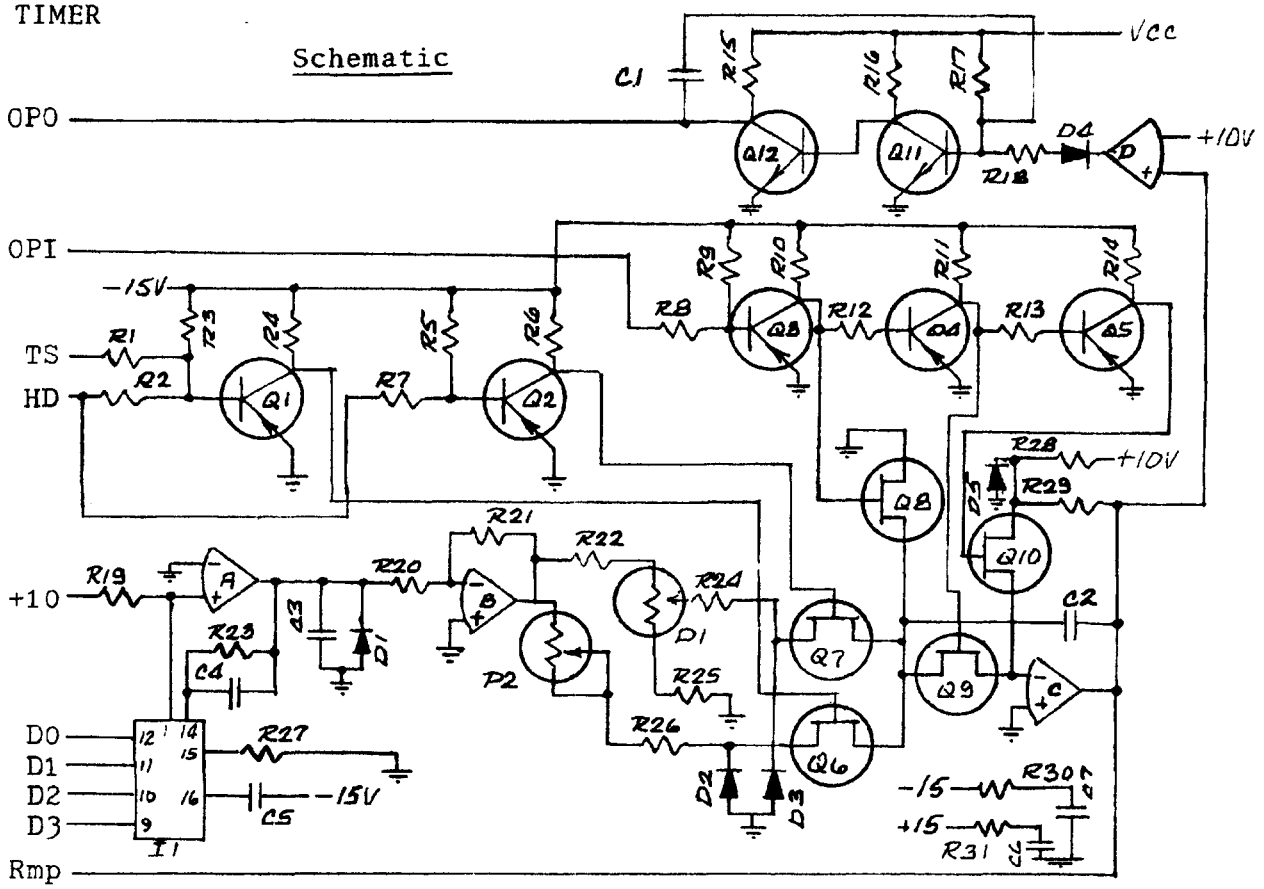
7986 CONTROL UNIT SCHEMATIC



7986 CONTROL UNIT ASSEMBLY DRAWING
980 TIMER CONNECTOR
CONTROL UNIT BUS
980 TIMER CONNECTOR
CONTROL UNIT BUS CONNECTOR
980 TIMER CONNECTOR
GND-
ROpb-
OPpb-
HDpb-
OPled-
HDled-
ROled-
ICled-
ICpb-
Vcc-
CLK-
A-
B-
C-
D-
0
A
Y
X
CTP
INT
B
8
1
2
3
4
5
6
7
9
IC
HD
DP
RO
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
I12
I13
I14
I15
I16
I17
Q1
Q2
Q3
Q4
Q5
P1
S1
S2
S3
A/B
%
Rmp-
D0-
D1-
D2-
D3-
Vcc-
OPO-
TS-
OPI-
HD-
AG-
+15-
DG-
+10-
-15-
DG
DG
X0
X2
X1
X6
X5
X4
MX
Y0
Y1
Y2
Y4
Y6
Y5
C0
OV
HD
OP
PS
TS
B0
B1
B2
B3
DG
Rmp
AG
Vcc
Vcc
AG
+15
+10
-15
Xo
Pot
Xs
Vcc-
ICpb-
ICled-
ROled-
HDled-
OPled-
HDpb-
OPpb-
ROpb-
GND-
A-
B-
C-
D-
CLK-

980 TIMER

Schematic



Parts List

R30,31	10	ohm
R15,27	4.7	K
R20,21,23,26	4.99	K*
R28,29	10.0	K*#
R1,2,4,6,7,8,10,11,14,16,18	15	K
R12,13	47	K
R25	49.9	K*
R3,5,9	100	K
R19,22	100	K*
R17	220	K
R24	1	M*
P1	50	K
P2	5	K

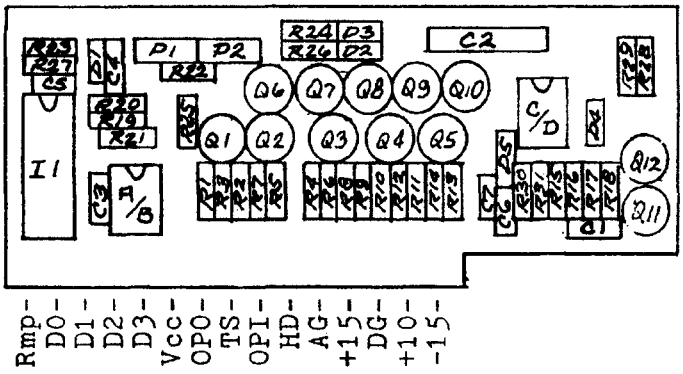
C5	.001	uf	cer.
C1	.022	uf	poly.
C4	.1	uf	cer.
C2	1.0	uf	poly.
C3	1.0	uf	tant.
C6,c7	6.8	uf	tant.

D1-D5	1N4148
(A/B)	MC1458
(C/D)	LF353
I1	LM1408N

D1-D5	1N4148
Q1-Q5	2N5138
Q6-Q10	2N5163
Q11-Q12	2N4124
(A/B)	MC1458
(D/D)	LF353
I1	LM1408N

* 1% metal film resistors
\# matched pair.

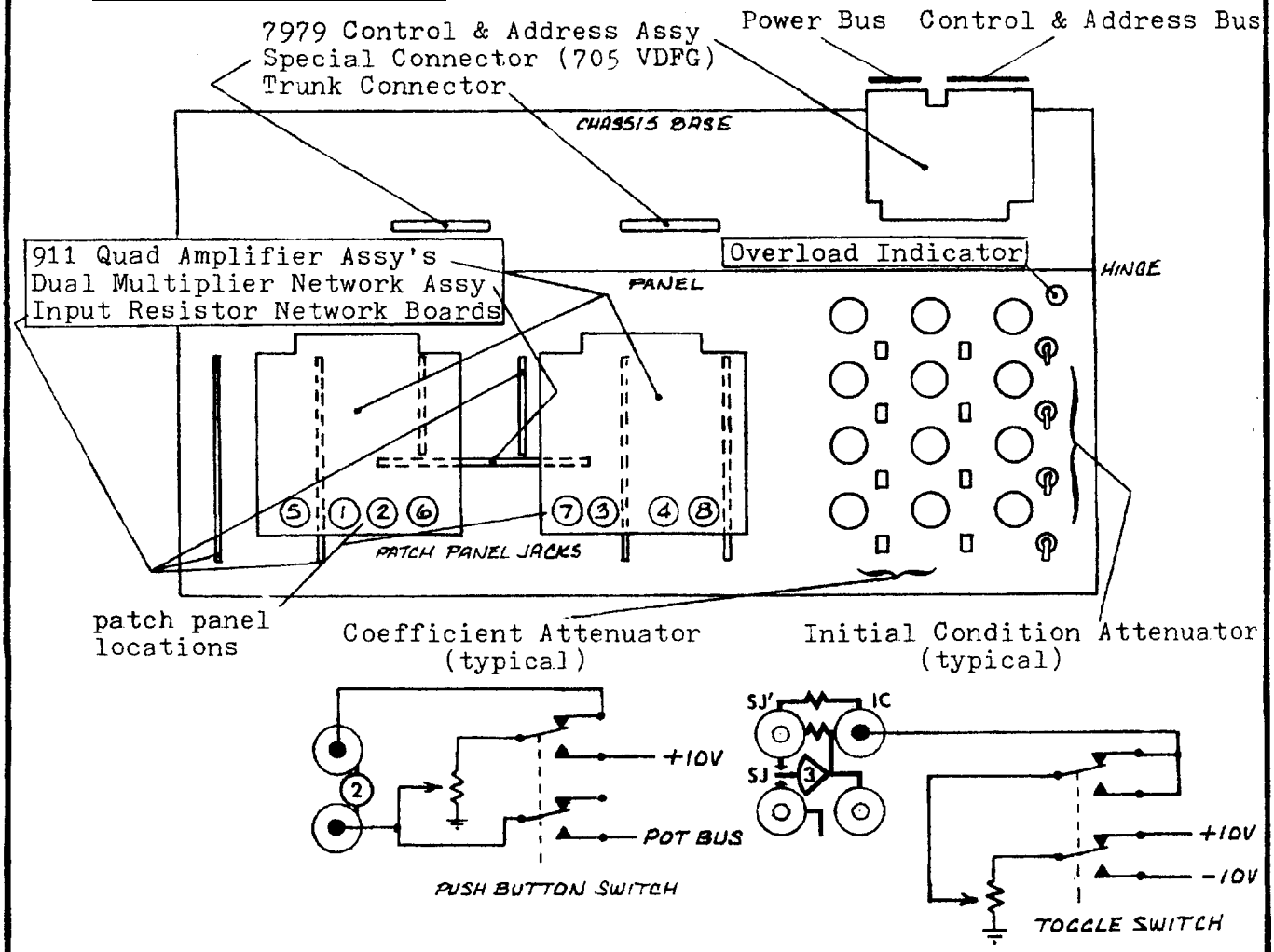
Assembly Drawing



GP-10 COMPUTING UNIT

The GP-10 computing unit performs the functions that are outlined by the patch panel layout of page 21 through use of the assemblies shown in the GP-10 system schematic.

GP-10 System Schematic



911 Quad Amplifier Assembly...Two identical PCB assemblies provide the eight patch panel amplifiers. Patch panel locations are shown on the GP-10 system schematic.

Input Resistor Network Boards...Amplifiers 1-6 have individual boards that connect the 50K and 5K patch panel input resistors. (It is noted that all 50K resistors have a 15K resistor from the input jack to ground. These resistors help to keep summing junction loading somewhat constant and thus minimize the effects of varying input loads. The 33pf compensation capacitor found on each summer-integrator board is placed across the SJ' feedback resistor.)

Integrator Initial Condition Attenuators...Amplifiers 1-4 have individual attenuators that are provided to enter integrator initial conditions. As shown on the typical circuit, each has a DPDT CO toggle switch that allows an operator to apply positive or negative initial conditions or to disconnect the attenuator.

Dual Multiplier Network...The multiplier network PCB plugs into the 10 pin connector, as shown on the GP-10 system schematic, with the components facing the top of the panel so that there is access to the adjustment potentiometers when the panel is in an open position.

External Function Generators...Function generator input jacks are provided amplifiers 7 and 8 as shown on the patch panel layout. Not a standard GP-10 feature, the function generators may either be located external to the GP-10 and terminated via the Trunk Connector or installed within the GP-10 as a special feature.

Coefficient Attenuators...The eight coefficient potentiometers are located on the panel as shown on the GP-10 system schematic. Each has a push button coefficient setting switch that, when depressed, replaces the patch panel input with reference and connects the wiper to the Pot Bus. The Pot Bus is connected via the 7979 Control and Address PCB to the Control and Address Bus.

Reference...Plus and minus 10 volts reference are provided by the Power Bus and trunked via the Control and Address PCB to the patch panel area.

Trunk Lines...The eight patch panel "TRUNKS" are terminated at the Trunk connector.

System Interface

Power...All power is provided by the Power Bus. Unregulated B+ and B- are regulated by the 7979 to provide the required +/- 15 volts. B+/B- is also regulated to provide the 24 volt relay supply. Plus/minus 10 volts and Vcc are provided by direct connections to the power bus.

Communication...All system interconnections are made via the Control and Address Bus.

Control...Mode control OP and HD produce the GP-10 negative logic OP. PS is buffered to be the 911 quad amplifier hold inhibit logic. TS is a switch control for the 24 volt relay logic.

Address...System address logic is decoded by two analog multiplixers where the analog outputs are connected to the Xout and Yout buses.

Pot Bus...The GP-10 pot bus is a direct connection to the Control & Address Bus.

OVLD.....The 7979 produces a logic alarm when any of the patch panel amplifier outputs exceed a positive or negative 10.5 volts.

OVLD BUS...The system OVLD BUS is pulled low.

LED Indicator...The LED located at the right corner of the panel is turned on.

CONTROL AND ADDRESS ASSEMBLY, 7979

The 7979 assembly connects a computing unit to the Control and Address Bus and the Power Bus. Included are the following functions:

1. Power Supply Regulation
2. Electronic Amplifier Address
3. Mode Control
4. Overrange Indication

1. Power Supply Regulation

Unregulated V+ and V- are regulated by I4 and I5 to produce the +15 and -15 volt supplies. V+ and V- are also combined and regulated by I3 to produce the +24 volt relay supply.

2. Electronic Amplifier Address

Two analog multiplexers (I1 and I2) decode the X and Y octal, amplifier selector codes (X0,X1,X2 and Y0,Y1,Y2.) Each multiplexer is enabled by a fixed connection to one of eight lines [X(0)-X(7) and Y(0)-Y(7)) which are the outputs of the decoded octal, computing unit selector codes (X4, X5,X6 and Y4,Y5,Y6.) The fixed connection gives a Control and Address Assembly a specific computing unit location within the 7000 address system. A code change can be made only by relocating the connection. The outputs of the two multiplexers are connected to Xad and Yad which are the analog address busses.

3. Mode Control

System mode control logic is buffered and conditioned to operate the computing unit's integrator switches and time scale relays. OP and HD logic inputs are conditioned by transistors Q11, Q10 and Q14 to provide the 0, -3v and -5v three level IC, HD and OP integrator switch control. The PS input by transistor Q9 provides HI, a voltage level to inhibit the hold mode switch for setting manual attenuators. TS logic by transistors Q8 and Q12 controls relay driver transistor Q13.

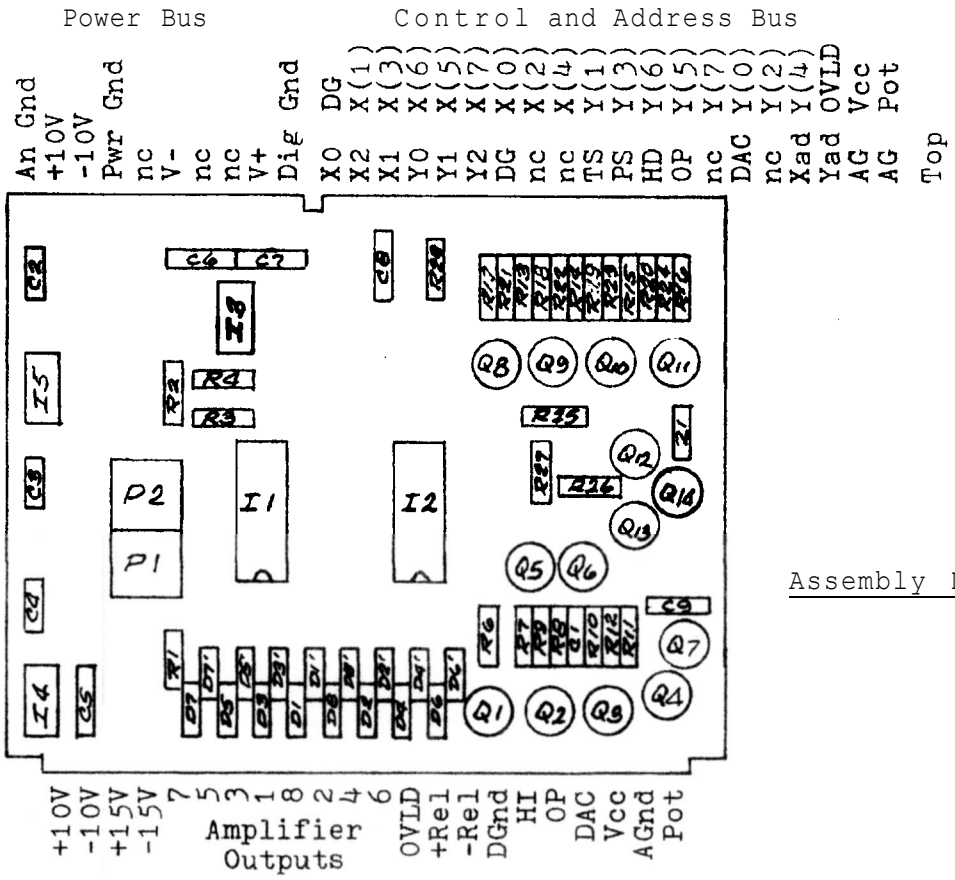
4. Overrange Indication

Eight computing unit amplifier outputs are diode gated to indicate when any one exceeds a positive or negative voltage bias. During an overrange condition transistor Q7 pulls the OVLD bus to ground. Parallel transistor Q4 is available to light an LED alarm that may optionally be added to the computing unit panel to show when any computing unit amplifier is in an overrange condition.

Adjustments

Overrange biases should be adjusted so that a plus or minus amplifier output of approximately 10.5 volts activates the overload indicator. P1 is the positive output bias adjustment; P2 is the negative bias adjustment.

7979 CONTROL AND ADDRESS ASSEMBLY



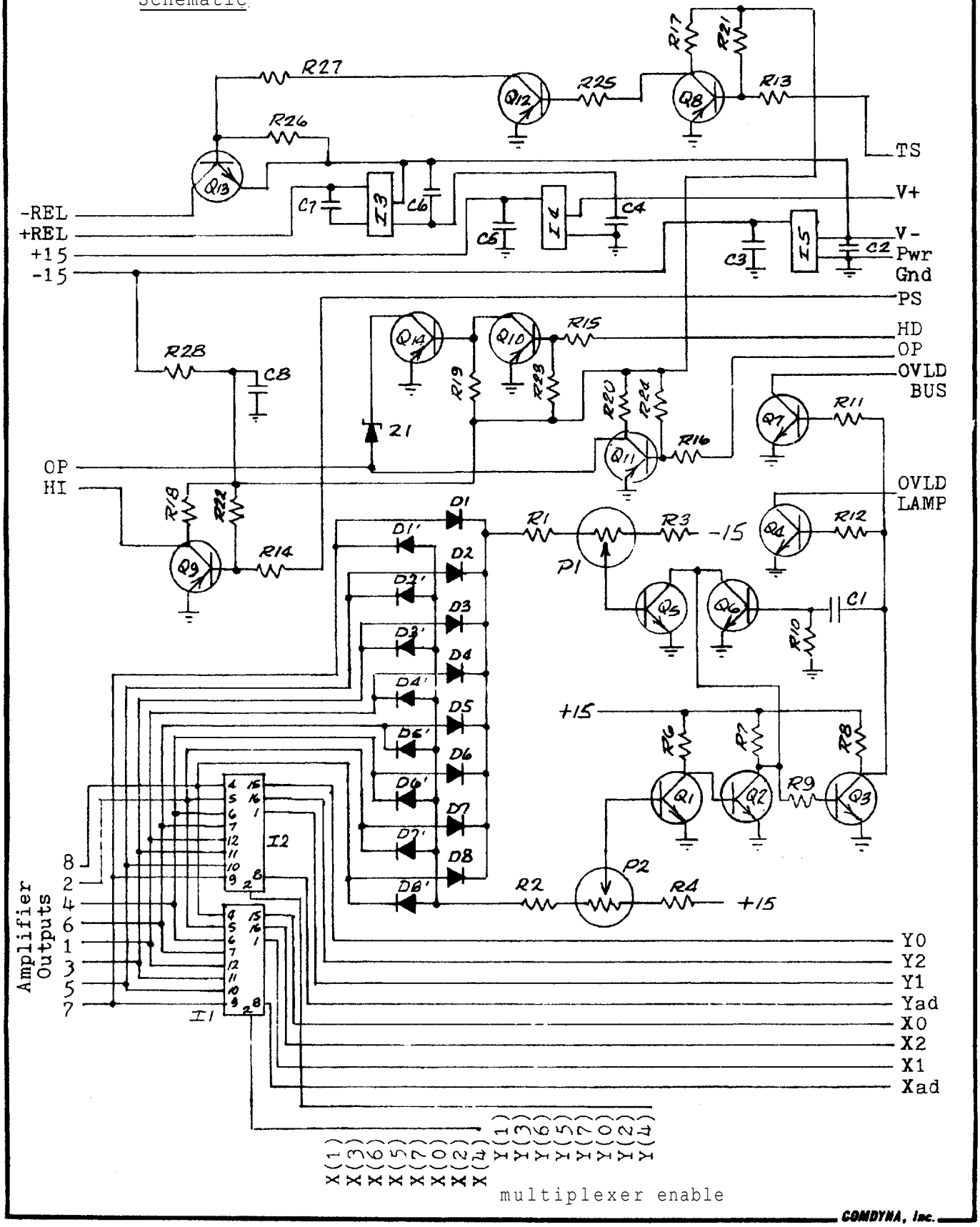
Assembly Drawing

Parts List

R28	10	ohm
R26	1	K
R12	5.6	K
R1,2,27	10	K
R3,4,11,25	15	K
R10,13-16	27	K
R6-9,17-20	47	K
R21-24	220	K
P1,P2	5	K
C5-7	.1 ufd	cer
C3	1 ufd	tan
C1	6.8 ufd	tan
C2,4,8	33 ufd	elec
D1-D8'	1N4148	
Z1	1N5226	3.3V
Q1-3,5-7	2N4124	NPN
Q8-12,14	2N4403	PNP
Q4,13	MPSA13	Dar
I1,I2	LF13508	MUX
I3	78M24	Reg
I4	7815	Reg
I5	7915	Reg

7979 CONTROL AND ADDRESS ASSEMBLY

Schematic



911-4 QUAD AMPLIFIER ASSEMBLY

The 911 board provides two single input, high gain operational amplifiers and two high gain operational amplifiers with electronic switch/integrator networks.

Amplifiers A and D are the single input amplifiers. Their patch panel summing junctions are connected directly to the inverting bases. Back-to-back diodes D2 and D3 offer protection by limiting summing junction potential. Capacitor C1 reduces peaking.

Amplifiers B and C are single input amplifiers with electronic switch/integrator networks. The electronic switches create two summing junctions, SJ and SJ'. When the switch control input (OP) is a logic 0 (ground or positive) summing junction SJ' conducts; when a logic 1 (more negative than -5 volts) summing junction SJ conducts.

The integrating capacitors are connected to the SJ summing junction so that an integrator is programmed by patching an amplifier output to a capacitor input. Two capacitor inputs (B and .1B) offer 10:1 time scale selection. The Time Scale Relay switches the time scale change (400:1) that is required for high speed repetitive operation. Where the repetitive operation feature is provided, the repetitive operation capacitors are connected directly to SJ. When the relay is energized, slow time capacitors are switched parallel the repetitive operation capacitors. (The relay is energized when an approximate negative 10 volts, not negative reference, is applied to the relay control input.)

Signal switching is performed by N-channel FET transistors Q6 thru Q8. Bipolar transistors Q1 thru Q5 are the FET switch drivers. 06 is the Hold FET (its an on resistance is less than 30 ohms to minimize summing errors.) Voltage divider resistors R8 and R12 are selected so that when OP is between -1 to -3 volts, Q6 shuts off; when OP is more negative Q6 turns on. Q7 is the shunt switch, Q8 is the SJ series switch and 09 is the SJ' series switch. Table 5-1 shows the switch states for the OP logic control voltage levels. N-channel FETs conduct with a zero gate voltage and shut off with approximately -7 volts. Back-to-back diodes D4 and D5 limit the SJ' potential when Q9 is off. Diodes D2 and D3 provide summing junction protection. D1 allows the Hold Inhibit control to override Q1 and turn Q6 on. (Hold Inhibit logic is applied in the Pot Set Mode to ground SJ summing junctions that would otherwise be floating.)

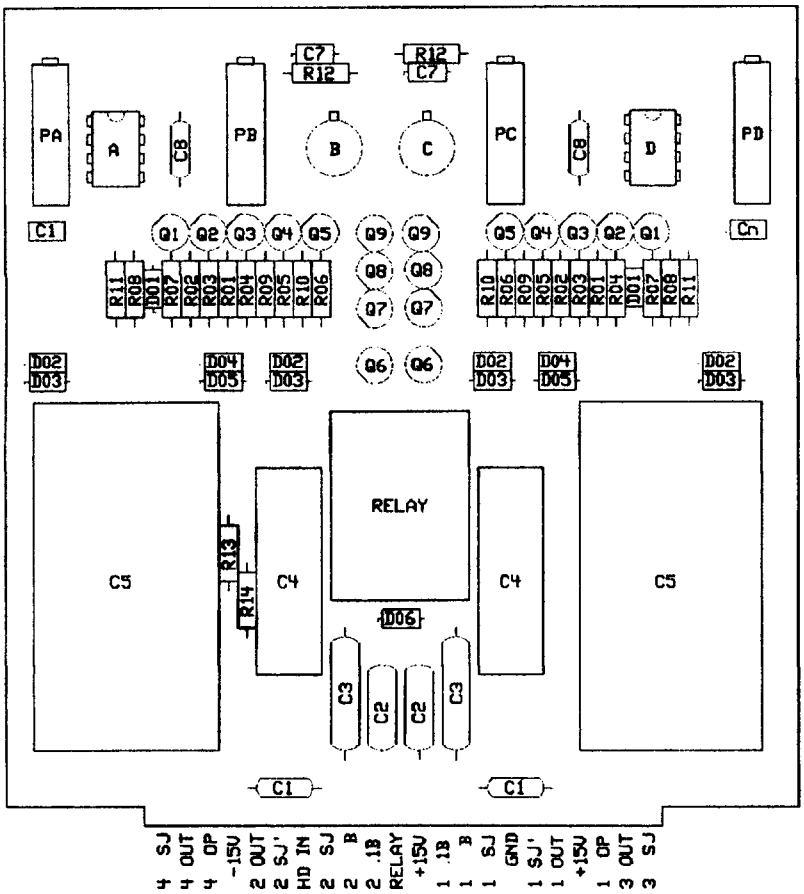
Capacitors C7 and resistors R13 provide amplifier compensation. Capacitors C1 reduces peaking when SJ has a resistor feedback. A similar capacitor is provided the SJ' summing jucntion.

BALANCING

To balance amplifiers A and D, patch resistor feedbacks and adjust potentiometers PA and PD until each amplifier output is a zero potential.

Amplifiers B and C should be balanced when programmed as integrators. Adjust PB and BC until each integrator produces a minimum integrator drift.

Assembly Drawing



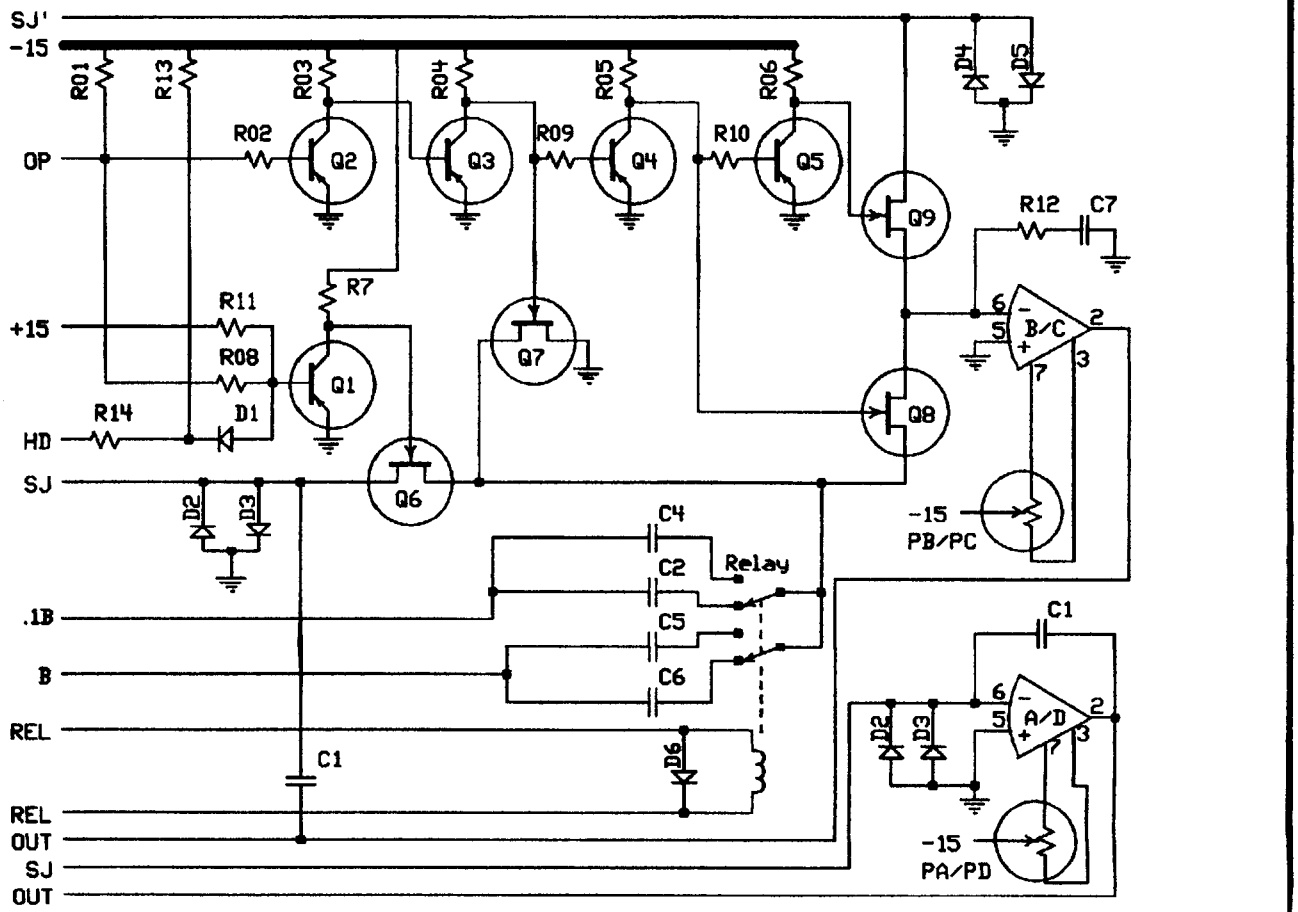
Parts List

R12	1	K
R14	2.2	K
R2 - R7	15	K
R1,R14	27	K
R8 - R10 . . .	47	K
R11	330	K
PA - PD	10	K
C1	15	pf
C2	.005	uf
C3	.05	uf
C4	2	uf
C5	20	uf
C6	0.1	uf
C7	500	pf
Q1 - Q5	2n4403	
Q6	2N4091	
Q7 - Q9	2N5485	
Amplifiers A,D	UA 741 CJG	
Amplifiers B,C	OP 97 EJ	
Relay	4A, 24V	

Table 5-1

OP LOGIC	Q6	Q7	Q8	Q9
OP > 0	OFF	ON	OFF	ON
-1V > OP > -3V	OFF	ON	OFF	ON
OP < -5V	ON	OFF	ON	OFF

Circuit Diagram



982/983 DUAL MULTIPLIER NETWORKS

The 982.2/983 board assemblies provide two independent multiplier networks, configured so that each, when used with an external operational amplifier may be programmed as a multiplier, divider, squarer or square root extractor.

Two inputs (Xin and Yin) are multiplied by integrated circuit M to produce a voltage proportional to the product X*Y. The voltage is converted to a current by resistor R5, scaled so that when connected to the summing junction of a patch panel amplifier, and where the feedback is a standard gain 150K ohm resistor, the amplifier will produce a full scale 10 volts output with 10 volts as the X and Y inputs.

Adjustments

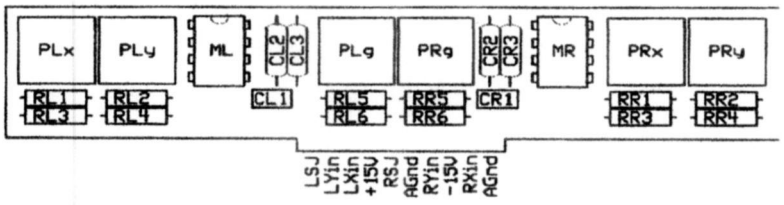
Each network is orginally adjusted at the factory. The networks should, however, be checked and readjusted, if necessary, during the initial checkout. Thereafter, the networks should be periodically checked to assure their most accurate operation. About 10 to 20 minutes should be allowed for warm-up before adjusting.

Adjustment consists of zero offset balancing (model 783 only) and a trim for gain and linearity. The suggested procedures are as follows:

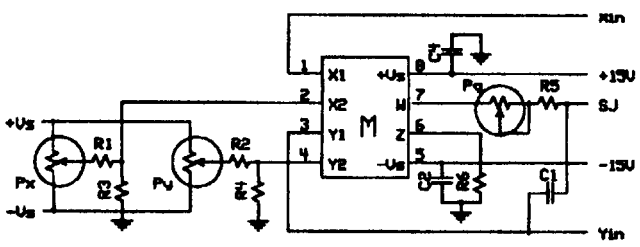
1. Program the network as a multiplier.
2. With inputs X and Y patched to ground, adjust potentiometer Pz for a zero output. Disregard for the 982.2 network.
3. Program an integrator as a ramp function to sweep from minus to plus 10 volts reference. (For convenience make all adjustments in the repetitive operation mode.) Display the multiplier output vs. the ramp input. Patch the ramp to the Y input; the X input should remain patched to ground. Adjust potentiometer Px until a best zero curve is obtained.
4. Reverse the X and Y inputs. Adjust potentiometer Py until a best zero error is obtained.
5. Readjust Pz if necessary.
6. Patch Reference (+ or -) to the X input and the ramp to the Y input. Sum the product with the correct polarity of the ramp to display an error curve. Adjust potentiometer Pg until a best error curve is obtained. Reverse the X and Y inputs, recheck and readjust if necessary. Check the error curve with the opposite polarity Reference input and reverse inputs as done with the original polarity. Trim potentiometer Pg until a best compromise of error curves is obtained for all four input combinations.

982.2 DUAL MULTIPLIER NETWORK

Assembly Drawing



Schematic



Parts List

R6	100	
R3, R4	1	K
R5	49.9	K
R1, R3	330	K
Px, Py	50	K
Pg	500	
C1	33	pf
C2, C3	.1	uf
M	AD633JN	

ACCESSORIES

ACCESSORIES, SYSTEM ORGANIZATION

The following are accessories installed on rack panel frames. Each frame may house two panel functions, designated left and right. In most cases, the frame functions will be connected and used with the GP-10 computing unit located directly below. Power is normally supplied via a cable from the primary chassis. Patched connections are normally terminated at the GP-10 Trunk Connector. In some instances, there will be permanent wiring between the GP-10 and rack frame. Also, it is also noted the GP-10 may be modified slightly to accommodate an accessory requirement.

709 Variable Diode Function Generators

If two VDFG panels are installed in a rack panel frame, the left is connected to the summing junction of amplifier 7, the right to amplifier 8. To use the DFG, patch a feedback resistor around the amplifier, the input to the FG jack. The amplifier output will be the DFG function.

Note: The VDFG's are always connected to the amplifier summing junctions; even with no patched input, the parallax will be present. In order to disable the VDFG's, the cable to the Trunk Connector must be disconnected.

705 Dual Variable Diode Function Generators

Referring to the 705 Board Layout, the "A" 705 is connected to the summing junction of amplifier 7, the "B" 705 to amplifier 8. Other than panel vs. screw driver adjustments, the 705 VDFG is used identically to the 709.

771 Transfer Function Simulator/717 Three Mode Controller

Either or both the above installed in a rack panel frame require use of a GP- 10 Trunk Connector, the terminations listed as follows:

Trunk 1	MODE CTL, common input bus
Trunk 2	717 OUTPUT
Trunk 3	717 FEEDBACK
Trunk 4	717 READOUT/system Pot Bus*
Trunk 5	NC
Trunk 6	NC
Trunk 7	771 INPUT
Trunk 8	771 OUTPUT

•The Computing Unit designated to accept a 717/771 is modified in that the POT BUS is permanently connected to Trunk 4. If the 717/771 cable is disconnected, Trunk 4 is not available for normal use.

Mode Control... To operate the 771/717 from the system mode control, patch OP to Trunk 1. Where the rack panel frame has two units, Trunk 1 is common to both.

717 Three Mode Controller...The 717 OUTPUT/FEEDBACK are patch cord connections to Trunks 2 and 3. As 717 READOUT bus is connected to the system POT bus, attenuator settings appear at the Control Unit DVM when a 717 coefficient set- up push button is depressed.

771 Transfer Function Simulator...The 771 INPUT/OUTPUT are patched connections to Trunks 7 and 8.

Although trunk connections are provided for operator convenience, connections may be patched directly to the panel jacks.

All rack panel accessories use system power (+15V, -15V, + 10V and -10V.) Panel AC power switches are thus removed.

450 SINE-COSINE FUNCTION GENERATOR

A GP-10 is modified for the Sine-Cosine DFG to be used with amplifiers 7 & 8. The angle 6 is patched to tie left FG input and is common to both Sine and Cosine functions. The sine function is the output of amplifier 7; the cosine is the output of amplifier 8. As with the 709/705 VDFG's, the Sine-Cosine inputs are always connected to amplifier 7 & 8 summing junctions. They can be disconnected only by removing the 450/705 PC boards.

Simple test cases for analog computer

① Two coupled linear algebraic equations

$$3x_1 + 4x_2 = -3$$
$$2x_1 + 5x_2 = +12$$

(solution is $x_1 = -9,\ x_2 = +6$)

Analog computer implementation:

$$x_1 = -\left(1 + \frac{4}{3}x_2\right) = -(1 + 1.33x_2)$$

$$x_2 = -\left(-\frac{12}{5} + \frac{2}{5}x_1\right) = -(-2.40 + 0.400x_1)$$

② Damped oscillator

ODE: $\ddot{x} + 2\zeta\omega_n\dot{x} + \omega_n^2 x = 0$

ICs: $\dot{x}(0) \equiv v_0,\quad x(0) = x_0$

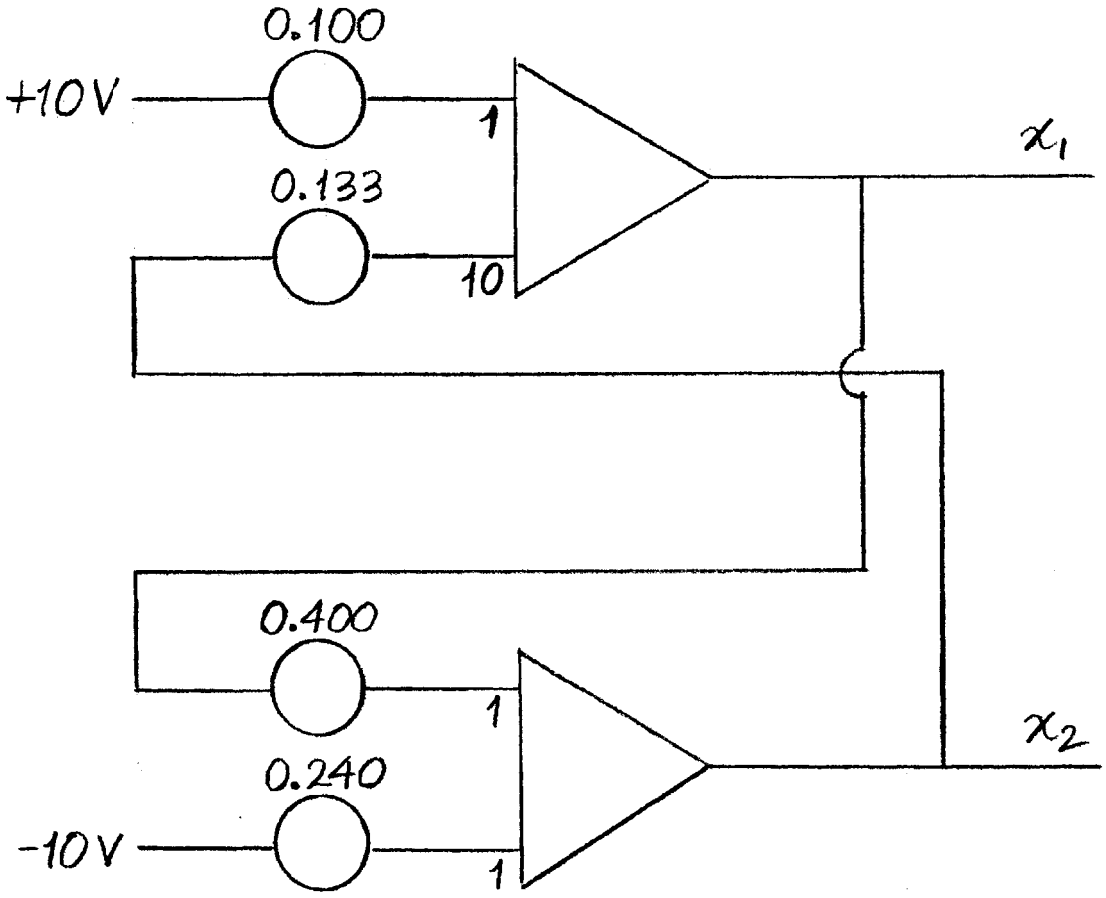
Analog computer implementation:

$$\frac{\ddot{x}}{\omega_n} = -\left(2\zeta\dot{x} + \omega_n x\right)$$

$$\dot{x}(t) = v_0 + \int_{\tau=0}^{\tau=t} \ddot{x}(\tau)\, d\tau$$

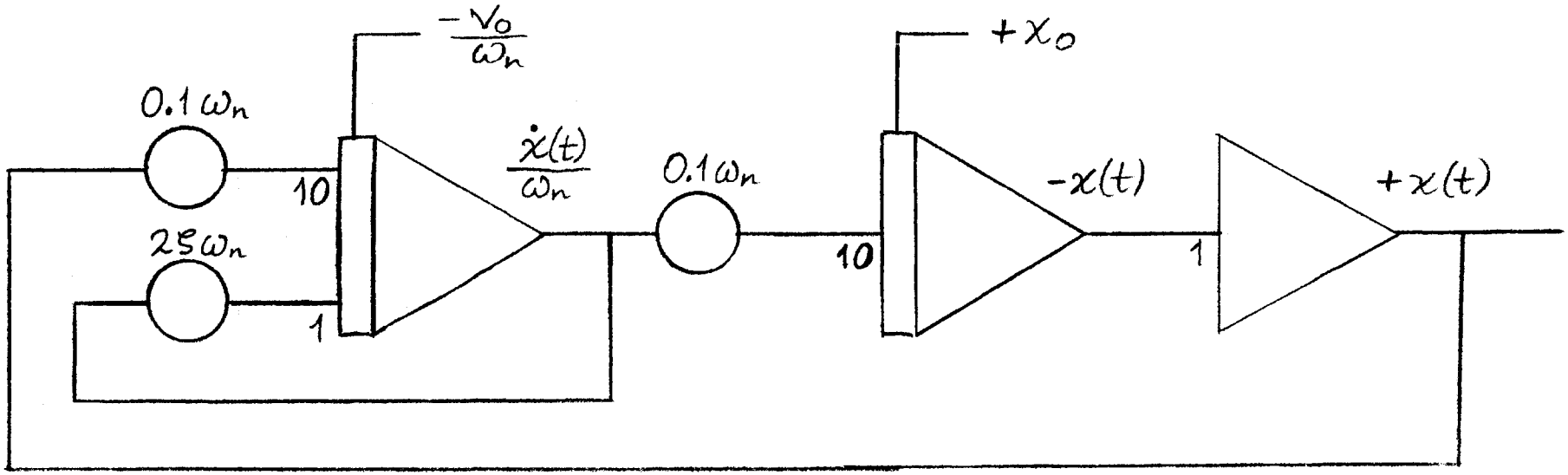
$$x(t) = x_0 + \int_{\tau=0}^{\tau=t} \dot{x}(\tau)\, d\tau$$

GP-10 circuit to solve coupled linear algebraic equations



GP-10 circuit for damped oscillator

Set coefficients and ICs in the IC mode, then switch to OP mode to produce time-dependent response.



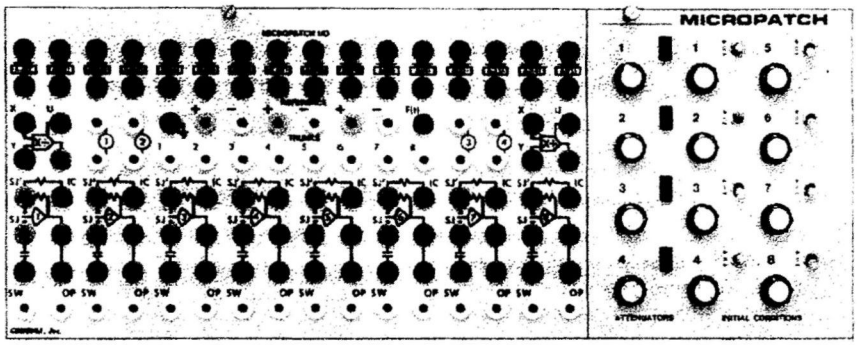
To make all three coefficient attenuation settings = 1, we can choose $\omega_n = 10$ rad/sec and $\zeta = 0.05$ ($\Rightarrow f_n = 1.59$ Hz $\approx f_d$).
In this case, we need not use the coefficient attenuators at all.
However, we still must use at least one IC attenuator for initial conditions.

COMDYNA, Inc.

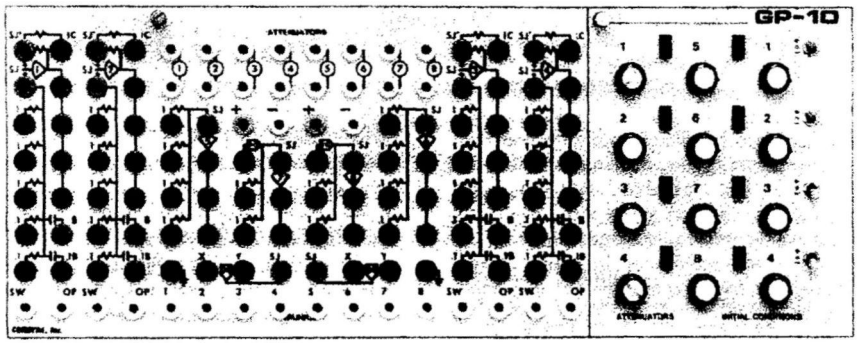
NEWS ITEMS

A NEW MODULAR, STACKABLE ANALOG/HYBRID COMPUTER

Micropatch, centerpiece, of the new 7000 Building Block analog/Hybrid computing system, replaces mechanical panels and patch cords with a digital computer controlled electronic switch network. Once programmed, Micropatch operates identically to traditional patch panel computers. Through a host digital computer, simulations are programmed directly from differential equation statements. From digital computer memory, stored simulation programs are instantly recalled for immediate use.



7000 ANALOG/HYBRID COMPUTING SYSTEMS



The availability of low cost analog multiplexers and digital interface devices has made electronic patching a practical reality. Taking advantage of recent integrated circuit developments, Micropatch is compatible and easily used with even the smallest microcomputers. For the first time, analog computers are programmed with common high level languages such as BASIC. PASCAL or FORTRAN. Treated as a digital computer peripheral, a Micropatch system can produce complex, nonlinear, high order simulations with only a few hundred bytes of a digital computer's usable memory.

Micropatch offers individuals not trained in the art of analog computer programming the opportunity to work with analog simulation models. From equations that are written in a state-variable form, a model is entered into the host digital computer via its keyboard/CRT. There the digital computer arranges equation statements into Micropatch switching commands, calculates coefficients and scales variables. Instantly the Micropatch is programmed and constants are entered. A simulation is ready to run only milliseconds after equation entry.

Convenient, unlimited program storage expands analog simulation into new dimensions of use. Once a model is digitally formatted it may be indefinitely stored. A virtual limitless number of analog models may be digitally stored and thus be available for instant use. An applications library can assume a live and accessible status as users may call simulations from a memory list. Interchange between libraries is encouraged as transfer can occur through written high level language statements or electronically through an exchange of discs or other mass storage devices.

A quick, useable access to a program library should enhance analog simulation's educational value. A keyboard entry is all that's needed to convert Micropatch into a physical system simulator. Through digital retrieval, one Micropatch system can become a chemical reactor, an automotive suspension, a non-linear vibrating membrane, a diseased heart, a servo controller or any physical phenomena that can be described with a set of ordinary differential equations. The simulation is perpetually on-call, ready for devotion to educational experiments. As patching and tedious program checkout are handled by the digital computer, a student spends virtually no time preparing the simulation for study

Quick recall of programs makes it feasible for a simulation, at any time, to be periodically analyzed. As frequently as desired, a researcher may retrieve and study a simulation. In the development of mathematical models frequent evaluations lay the foundations for minds to transform intuitive understandings into analytical derivations. Modifications, parameter changes and interactions with a model are the ingredients for successful math model developments. Micropatch's accessibility for repeated studies is expected to hasten the creation and validation of system models.

Once a model is declared valid, quick recall expands application possibilities. Analog simulations have proven records in product design, the selection of equipment or components, the development of operating procedures, the evaluation of safety considerations, the treatment of diseases and the optimization of processes. Convenient program storage will expand these proven application areas and open the door for analog simulation's entry into new and related fields of use.

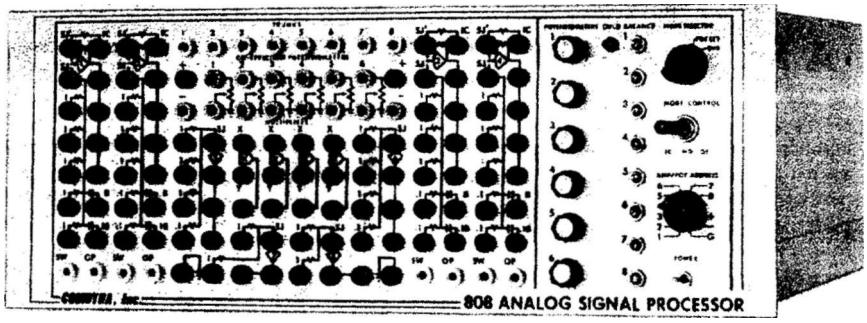
A major Micropatch design feature is that electronic patching is provided without sacrificing the versatility of traditional analog computers. All the non-linearities, discontinuities and empirical functions that analog computer programmers so artfully incorporate into simulations are equally within Micropatch's capabilities. Advanced operational techniques can be implemented if the programmer chooses.

The full range of analog computing functions is met with a combination of patch panel and electronic patching. Certain electronic switch terminations are brought to a patch panel where analog functions may be applied. Once a function is patch-

. . . continued on back page

GROWTH IN COMBINED UNIT SIMULATION SYSTEMS

An increasing number of organizations are finding that combined 808 Analog Signal Processors provide an excellent means of meeting medium and large simulation requirements. Six or more low cost 808 units, mounted into a standard electronic enclosure, can be operated by one 985 Control Unit. Linear and non-linear simulations requiring in excess of 50 amplifiers are well within the combined unit capacity.



808 Analog Signal Processor

Some of the more recent installations are given below:

- — Sperry Flight Systems, Phoenix, AZ
- — Sperry Avionics, Phoenix, AZ
- — Aerojet Strategic Propulsion Company, Sacramento, CA
- — Johns Hopkins University, Baltimore, MD
- — Bendix Corporation, N. Hollywood, CA
- — Hughes Aircraft Company, El Segundo, CA
- — TRW, Inc., Redondo Beach, CA
- — Boeing Corporation, Seattle, WA
- — General Electric Company, Evendale, OH
- — Grumman Aerospace Corporation, Beth page, NY

NEW COMPUTER... *cont. from front, page*

ed, if then is incorporated into the electronic switch network. By mixing patched functions with electronic programming, a Micropatch system can be arranged to meet a variety of computing requirements.

Micropatch is one of two 7000 Building Block units. The other is the model GP-10 traditionally patched analog computer. A 7000 system may be composed of one or more of either or a combination of both. Modular and stackable, Micropatch and the GP-10 are the building blocks that provide the flexibility needed to efficiently construct simulation systems. Each may be operated alone for small applications or blocked together to meet practically any sized requirement. Systems may begin small and grow as demands increase. Large systems may be disassembled into smaller ones. The building block organization lets purchasers buy no more equipment than is necessary to handle the job.

Structured much like the Comdyna GP-6, each GP-10 computing *unit handles* up to fourth order simulations, has four time scales per integrator, a full complement of non-linear elements and utilizes GP-6 accessories. Also like the GP-6, the GP-10 offers quality analog computing at a low cost. Inclusion of GP-10 units into a 7000 system provides the opportunity to minimize the overall cost per operation. A blend of the GP-10 with Micropatch yields the best possible cost effective system.

To mix electronic and patched programming, Micropatch utilizes a transfer function approach to handle the terms of a differential equation model. Each term of a state variable equation is treated as an input/output function of a variable or variables. Whether a term is linear, nonlinear, simple or complex, it is viewed by the programmer as a transfer function. Inherent to the basic Micropatch switching network are the combined functions of sign determination and multiplication by a constant. These are the basic Micropatch transfer functions. Equations with terms having only these operations are limited to linear simulations. To produce other functions, the basic linear operations must be combined with operations that are created through patched techniques. To include a patched function:

1. A term's variable is electronically directed to a specific panel output location.
2. The selected variable is conditioned by patched operations.
3. The conditioned variable is patched to a specific Micropatch panel input location.
4. The input is electronically given a designated sign, digitally attenuated and connected as one term of a selected equation.

In addition to its programming versatility, a major strength of the 7000 Series is its strong capabilities to interact with digital computers. Distinguishing features include an ail electronic amplifier address, analog/digital and digital/analog conversion and an interface for bidirectional digital computer data transfer. As a hybrid computer, the 7000 may be operated entirely from the host digital computer as well as from a desk top control module.

Although most attention will likely focus on the unique, electronic patching network, we believe that the most powerful feature of the 7000 Building Block Series is its adaptability to meet a diversity of analog/hybrid computing requirements. Whether small or large, patch cord or electronically programmed, a system can be structured for every budget and need.

7000 literature is to be available by June 1981. Initial installations are to occur during early summer of 1981.

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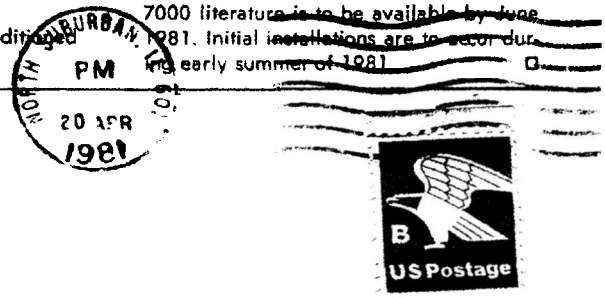
305 Devonshire Road Barrington, Illinois 60010



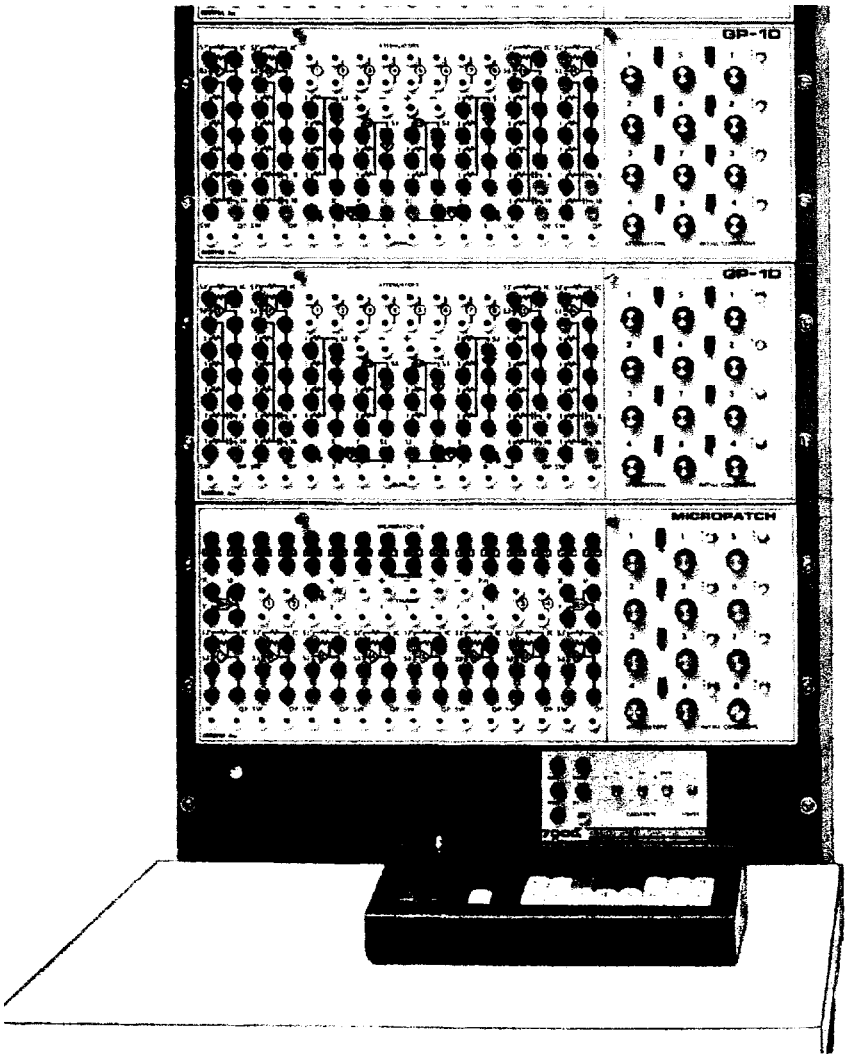
May 1983

SIMULATOR TIE-INS... an aid to control systems development

In the analysis of control designs there is often a need to test and develop physical components in a working environment. As the electrical analogs of real apparatus, analog simulators provide such environments. Where parts or ail of actual facilities can be replaced by a simulator tie-in, a physical component can be tested under realistic but predictable operating conditions.

Comdyna 7000 analog/hybrid computer systems are designed for tie-in applications. They are accurate, inexpensive and can be configured to the exact size of a simulation requirement. Mountable into an electronic rack or enclosure, a 7000 simulator is quickly integrated into laboratory facilities. Good trunking enables signals to be easily transported to and from instrumentation and control devices. A large and sturdy patching area of standard banana plugs and jacks facilitates the programming of simulation models and their tie-in with physical equipment.

7000 simulators are also designed for easy tie-in to microcomputing systems. Standard models offer a microcomputer interface with an instruction set for multiplexing analog variables and converting the variables to digital data. With the MICROPATCH option analog simulation programs can be electronically patched and digitally stored. With the multiplying digital/analog converter expansion, simulation parameters may be digitally set and controlled by microcomputer programs.

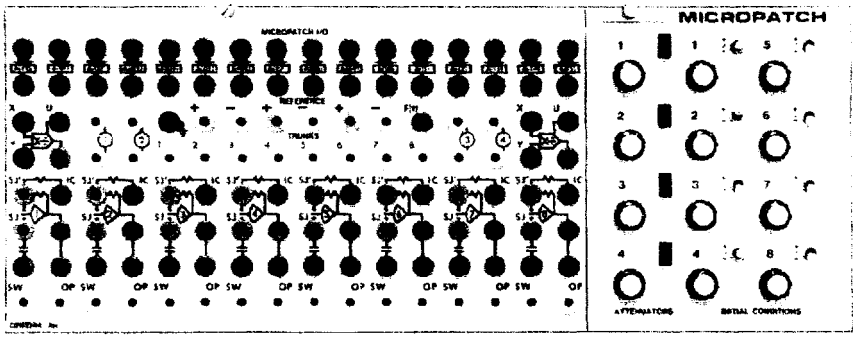


The 7000 Analog/Hybrid Computing Systems offers a building block construction that can be configured to specific simulation requirements.

MICROPATCH... now available for the Apple II

MICROPATCH programs can now be formatted, stored and executed with the Apple II processor. By entering a set of state-variable differential equations into the Apple, a MICROPATCH program can be electronically patched for immediate use as a pure analog computer simulation or as an Apple based hybrid computer simulation. Once formatted, the MICROPATCH program can be stored and recalled with use of the Apple's disc and controller.

While the Apple package offers plug-in convenience, the software is not limited to the Apple processor. Written in BASIC, the program is easily transferred to other computers. With the entry of a few machine language routines, the BASIC program of any microcomputer can be utilized.



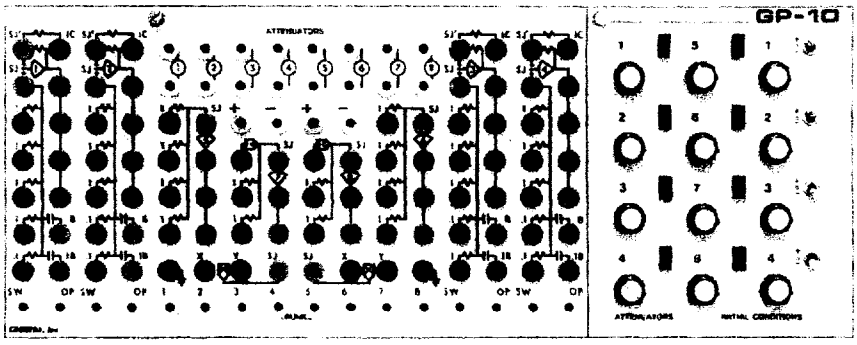
MICROPATCH is a computing unit of the 7000 Analog/Hybrid Computing Systems. It operates identically to traditional analog computers except that an electronic switching network replaces patch cord programming and digital computer storage replaces mechanical patch panels. MICROPATCH simulations have the same hands-on benefits as patch panel computer simulations. They can be tied into physical equipment or used as stand-alone simulators.

May 1983

DATA ACQUISITION WITH THE GP-10

Small analog computers are highly useful to digital data acquisition programs. Simple patch panel functions can reduce software requirements, increase operating speeds and add parallelism to signal processing. Analog computer variables are voltage signals like raw measurements but they are superior for conversion and handling by the digital computer.

The GP-10 analog computing unit offers an inexpensive and convenient addition to a digital data acquisition facility. The GP-10, with microcomputer interface, is a complete data acquisition system. No matter what type of conversion is used, the GP-10 analog unit provides front end operations that include general purpose filtering, signal conditioning and arithmetic manipulation of instrumentation variables. Operations that would otherwise burden the digital computer program can often be handled with a few analog panel connections.



As a complete data acquisition unit, the GP-10 plugs into a microcomputer I/O bus. Microcomputer routines multiplex the analog computer variables, control the analog/digital converter and sense single bit logic states. The universal parallel interface port is adaptable to all microcomputer models. A standard interface with software is available for the Apple II.

Where the applications concern both data acquisition and control, digital/analog converters can be included. The user thus has the options to construct continuous controllers from analog patch panel components, utilize digital control with either voltage or multiplying digital/analog converters or apply state control with the interface unit's single bit outputs.

From a selection of computing and interface options, a GP-10 can be custom configured to meet a wide range of signal handling needs. Prices start under $1,000.

ANALOG COMPUTER HANDBOOK

The text and laboratory work book, written by Dr. Violet B. Haas, Electrical Engineering Department, Purdue University, has been published by Publications Press, P.O. Box 1998, Bloomington, IN, 47402. Books may be purchased directly from the publisher or from Comdyna, Inc. at $9.00 each.

Dr. Haas developed the handbook for use in an undergraduate controls program. Material and experiments cover analog computer programming, dynamic systems simulation and fundamentals of control theory. All experiments can be handled with the Comdyna GP-6 analog computer.

HYBRID PHARMACOKINETICS

Pharmacokinetics simulations are now being performed on a hybrid computing system that consists of the GP-10 analog simulation unit and Apple II microcomputer. in the simulation of drug absorption, distribution and elimination in the body, the Apple inputs the simulated drug regimens and monitors digitized drug concentrations.

Analog simulations have proved useful in the research, education and clinical application of pharmacokinetics models. The inclusion of a central processor has added the capabilities to store and retrieve patient data, perform statistical analyses, compile reports and aid the deployment of drug models. All the benefits of analog computer simulation regarding the development of mathematical models and prediction of patient drug doses has been maintained or enhanced.

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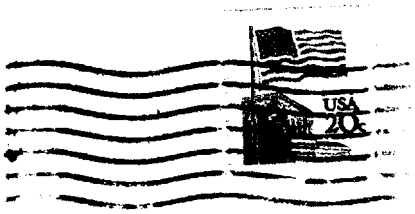

December 1984

PRICE SHEET

COMDYNA, Inc

Each Comdyna analog/hybrid computer that is included herein is priced by adding options and features to a basic configuration. Section A that follows lists general accessories that may be used with all or most systems and do not require installation at the time of the system's purchase.

WARRANTY

All products are covered by a one year warranty. In event of an operational defect, the product will be repaired by either replacing the defective part or repaired at the factory, at no cost, providing that the defect is not the result of abuse. The warranty covers defects in workmanship and all electronic malfunctions.

SEVEN DAY CONSIGNMENT - EVALUATION PURCHASE

Purchase orders may be accepted on a seven day consignment-evaluation basis. On this basis, one standard system will be consigned to purchaser for a seven day evaluation period. After the seven day period, the unit is either accepted or it may be returned and the purchase order cancelled. Consignee is to be responsible for the unit's safekeeping during the period and for shipping charges. To be effective, the purchase order must state "Seven Day Consignment-Evaluation."

DESCRIPTION	QTY	UNIT	EXT
7000 ANALOG/HYBRID COMPUTING SYSTEMS			
Primary System			
Chassis *completely wired does not include power supply or 7976 interface network.*		$ 125	
Desk top 7003 (single computing units only)		125	
Rack Mount, 7013 (single or multiple units)	select one . . . . 1 ea.		_____
Power Supply			
Low Current, 7116 (single units)		95	
Medium Current, 7117 (2-4 units)		145	
High Current, 7118 (5-8 units)	select one . . . . 1 ea.	195	_____
Interface Network, 7976 *required tor Micropatch and for use of 7986 control unit or external digital computer.*	optional . . . . 1 ea.	175	_____
Control Unit 7986 *requires 7976 network*	optional . . . . 1 ea.	675	_____
Analog/Digital Converter, 7093 *12 bit w/8 bit DAC curve generator*	optional . . . . 1 ea.	345	_____
Microcomputer Connecting Cable see *Section A*	optional . . . . 1 ea.		_____
COMPUTING UNITS			
GP-10 Basic *inc. wired chassis, 2* ea. *911 quad amp, grps., patch cord set.*	quantity . . . . ___ea.	895	_____
Control and Address Group, 7979 *requires 7976 interface network.* (1 per basic)	optional . . . . ___ea.	165	_____
Integrating Capacitor Group *1:1, 10:1, 400:1 and 4000:1 time* scales. (1 per basic)	optional . . . . ___ea.	250	_____
Dual Multiplier Network *see Section A* (1 per basic)	optional . . . . ___ea.		_____
Alternate integrating Capacitor Groups			
1:1 Time Scale, 7171		115	_____
10:1 Time Scale, 7172		55	_____
400:1 Time Scale, 7173		40	_____
4000:1 Time Scale, 7174		40	_____

DESCRIPTION		QTY	UNIT	EXT
MICROPATCH Basic *inc. wired chassis, 1 ea. 7979 control/ address, 1 ea. 7912 quad integrator, 1 ea. 7975 quad switch, patch cord set*	quantity	___ea.	1935	_____
Quad integrator, 7912 (expansion 1 per basic)	optional	1 ea.	345	_____
Attenuator-Switch Group, 7975 (expansion 1-3 per basic)	optional	___ea.	795	_____
Attenuator-Switch Group, 7975A *alternate to 7975, same except attenuators are 12 bit resolution.*	optional	___ea.	945	_____
Dual Multiplier/Divider, 7282 *1 % FS accuracy* (1 per basic)	optional	___ea.	170	_____
Alternate multiplier, 0.5% *accuracy*	add		100	_____
Alternate multiplier, *0.1% accuracy*	add		275	_____
Patch Cord Set, 7840 (additional patch cords for expanded unit)	optional	___ea.	60	_____
MULTIPLYING DIGITAL/ANALOG CONVERTERS				
Eight Channel Assembly, 796 *ten bit resolution, printed circuit board, used with 7976 interface.*	quantity	___ea.	650	_____
Eight Channel Assembly, 796A *same as 796 except resolution is twelve bits.*	quantity	___ea.	795	_____
Installation in Comdyna computing units *consult factory*				
Patch Panel and Chassis, 796C *Rack mountable chassis, completely wired for patched inputs and outputs of two 796 MDAC assemblies.* (1 per two 796 assemblies)	optional	___ea.	195	_____
GP-6 DESK TOP ANALOG COMPUTER				
Inc. standard eight amplifier basic unit, slow time and repetitive operation feature, digital voltmeter readout, dual multiplier network-1% accuracy, patch cord set and microcomputer interface connector.	quantity	___ea.	1845	_____
Alternate multiplier, 0.5% *accuracy*	add	___ea.	100	_____
Alternate multiplier, *0.1% accuracy*	add	___ea.	245	_____
Cassette Training Program, 101	quantity	___ea.	55	_____
Tutor Cassette Player, 615	quantity	___ea.	95	_____
MICROHYBRID I INTERFACE UNIT				
Standard Basic Unit *inc. fully wired chassis, asynchronous logic functions, sixteen channel multiplexer, patch cord set, GP-6 connecting cable.*	quantity	___ea.	1075	_____
I/O Port, 932, (one per basic)	optional	___ea.	80	_____
Quad Amplifier Group, 911 (one per basic)	optional	___ea.	130	_____
Dual Downcounter Group, 938 (one per basic)	optional	___ea.	115	_____
Analog/Digital Converter *see below* (one per basic)	optional	___ea.		_____
Multiplying Digital/Analog Converter see *below* (one-four per basic)	optional	___ea.		_____
Microcomputer Connecting Cable see Section A (one per basic)	optional	___ea.		_____
766 INTERFACE UNIT				
Basic Unit *inc. desktop chassis, GP-6 connecting cable, eight channel multiplexer, flat cable for 24 bit parallel I/O*	quantity	___ea.	250	_____
Microcomputer interface options (one per basic)				
Apple II	optional	___ea.	95	_____
Other Microcomputer Models *(consult factory)*	optional	___ea.		_____
Analog Digital Converter *see below* (one per basic)	optional	___ea.		_____
Multiplying Digital/Analog Converter *(see below)* (one or two per basic	optional	___ea.		_____

DESCRIPTION		QTY	UNIT	EXT
Converters for Microhybrid I and 766 Interface				
Analog/Digital, 7091 *8 bit plus sign*	....		95	
Analog/Digital, 7093 *12 bit plus sign and includes 8 bit DAC curve generator.*	....		345	
Multiplying Digital/Analog, 937 *8 bit resolution*	....		75	
Multiplying Digital/Analog, 935 *12 bit plus sign resolution*	....		125	
808 ANALOG SIGNAL PROCESSOR				
Basic Unit *inc. fully wired rack mount chassis, two 911 quad amplifier groups but without integrating capacitors, patch cord set*	quantity	ea.	995	
Expanded Integrating Capacitor Set *inc. four 1:1, 10:1, 400:1 and 4000:1 time scale integrating capacitors with time scale relay.*	optional	ea.	250	
Dual Multiplier Network *see Section A* (one or two per basic)	optional	ea.	—	
809 ANALOG SIGNAL PROCESSOR				
Basic Unit *inc. fully wired rack mount chassis, two 911 quad amplifier groups but without integrating capacitors, card programming facilities.*	quantity	ea.	995	
Integrating Capacitors see *below* (one or two sets per basic)				
Dual Multiplier Network *see Section A* (one or two per basic)	optional	ea.	—	
General Program Card, model 400	optional	ea.	25	
Amplifier Balance Program Card, model 410	optional	1 ea.	32	
Control Connector *male 10 pin*	optional	ea.	7	
General Programming Kit	optional	ea.	45	
Integrating Capacitors for 809 and alternates for 808				
1:1 Time Scale		ea.	115	
10:1 Time Scale		ea.	50	
400:1 Time Scale		ea.	40	
4000:1 Time Scale		ea.	40	
Other time scales consult factory				
CONTROL UNIT, MODEL 785				
Organizes up to *six 808/809 Analog Signal Processors into a single operating system, inc. digital voltmeter readout, slow and fast time base, repetitive operation timing unit, push button mode control and amplifier address switches.*	quantity	ea.	750	
MATH MODEL SIMULATOR				
Self-contained instructional package inc. complete Math Model Simulator and "Introduction to Systems and System Simulation" text and laboratory work book.	quantity	ea.	495	
Analog/digital and Digital/analog Converter Expansion *eight bits including sign with Apple II connecting cable.*	optional	ea.	195	
SECTION A (ACCESSORIES AND GENERAL OPTIONS)				
MULTIPLIER/DIVIDERS				
Multiplication/division accuracy is selected from a choice of three dual multiplier networks. The plug-in assemblies may be field installed and exchanged on a full credit basis to upgrade existing systems.				
Dual Multiplier Network, 782-1 *1% full scale accuracy*	....		150	
Dual Multiplier Network, 782-.5 0.5% *full scale accuracy*	....		250	
Dual Multiplier Network, 783- *0.1% full scale accuracy*	....		395	

DESCRIPTION	QTY	UNIT	EXT
SECTION A (ACCESSORIES AND GENERAL OPTIONS)			
SIMULATION SUB-SYSTEMS			
The following may be furnished in either desktop or rack mounting housings			
Variable Diode Function Generator, 701 eleven segments, fixed breakpoints	quantity	ea. 165	
Variable Diode Function Generator, 709 eleven segments, variable breakpoints	quantity	ea. 205	
Transfer Function Simulator, 771 inc. power supply	quantity	ea. 350	
Three Mode Controller, 717 inc. power supply	quantity	ea. 350	
Attenuator Expansion Group, 731 inc. seven potentiometers with push button coefficient setting switches.	quantity	ea. 250	
The following are printed circuit assemblies.			
Variable Diode Function Generator, 705 Dual channels, eleven segments each, variable breakpoints, screw driver set adjustments.	quantity	ea. 350	
Sine-Cosine Input Card, 450 signal shaping input for 705 VDFG, enables VDFG to produce 360 degree sine-cosine functions.	quantity	ea. 125	
MICROCOMPUTER INTERFACE CABLES			
Apple II plugs into peripheral connector	quantity	ea. 150	
TRS-80plugs into parallel port	quantity	ea. 170	
AIM 65 plugs into parallel port	quantity	ea. 180	
Other microcomputer models consult factory.			
BANANA PLUG MODULES AND ELEMENTS			
D/A Electronic Switch, 9302	quantity	ea. 35	
Comparator Feedback Element, 9390	quantity	ea. 12	
Single Pole, Double Throw Function Switch, 9408	quantity	ea. 22	
Coefficient Attenuator, 9447	quantity	ea. 25	
Adjustable Hard Limiter, 9517	quantity	ea. 40	
Zero Limiter, 9528	quantity	ea. 20	
Adjustable Dead Space, 9520	quantity	ea. 35	
Absolute Value, 9560	quantity	ea. 49	
Hysteresis, 9570	quantity	ea. 75	
3 Input Summer Network, 9700	quantity	ea. 21	
Patchable Diode, 9780	quantity	ea. 10	
PROGRAMMING AND LEARNING AIDS			
"**Analog Computer Handbook**" by Dr. Violet B. Haas a laboratory text and work book.	quantity	ea. 9	
PATCHING AIDS			
Pamona Shorting Plug	quantity	ea. 3	
Stack-up Patch Cords 5, 8 or 12 inch lengths	quantity	ea. 4	
Stack-up Patch Cords custom length	quantity	ea. 8	
Patch Cord Kits 44 patch cords: 5, 7, 10, 12 inch lengths	quantity	ea. 85	
220 VOLT OPERATION add per system	quantity	ea. 35	

October, 1982

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