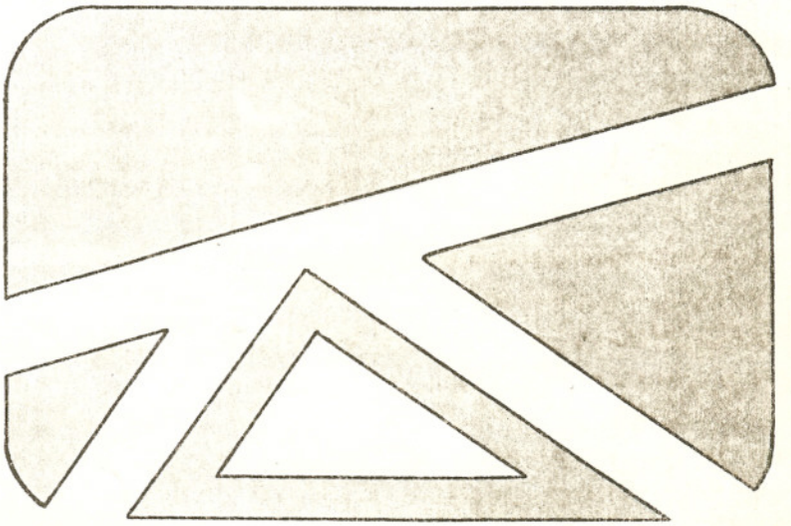
MPU-B



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FULCRUM (EUROPE)
VALLEY HOUSE
PURLEIGH
ESSEX, ENGLAND CM3 6QH
TELEPHONE: (0621) 828763

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MPU-8

MPU-B

8085-BASED MICROPROCESSOR

GENERAL

The IMSAI MPU-B board contains several distinct components. The block diagram shows these components and their interaction. The major components are listed:

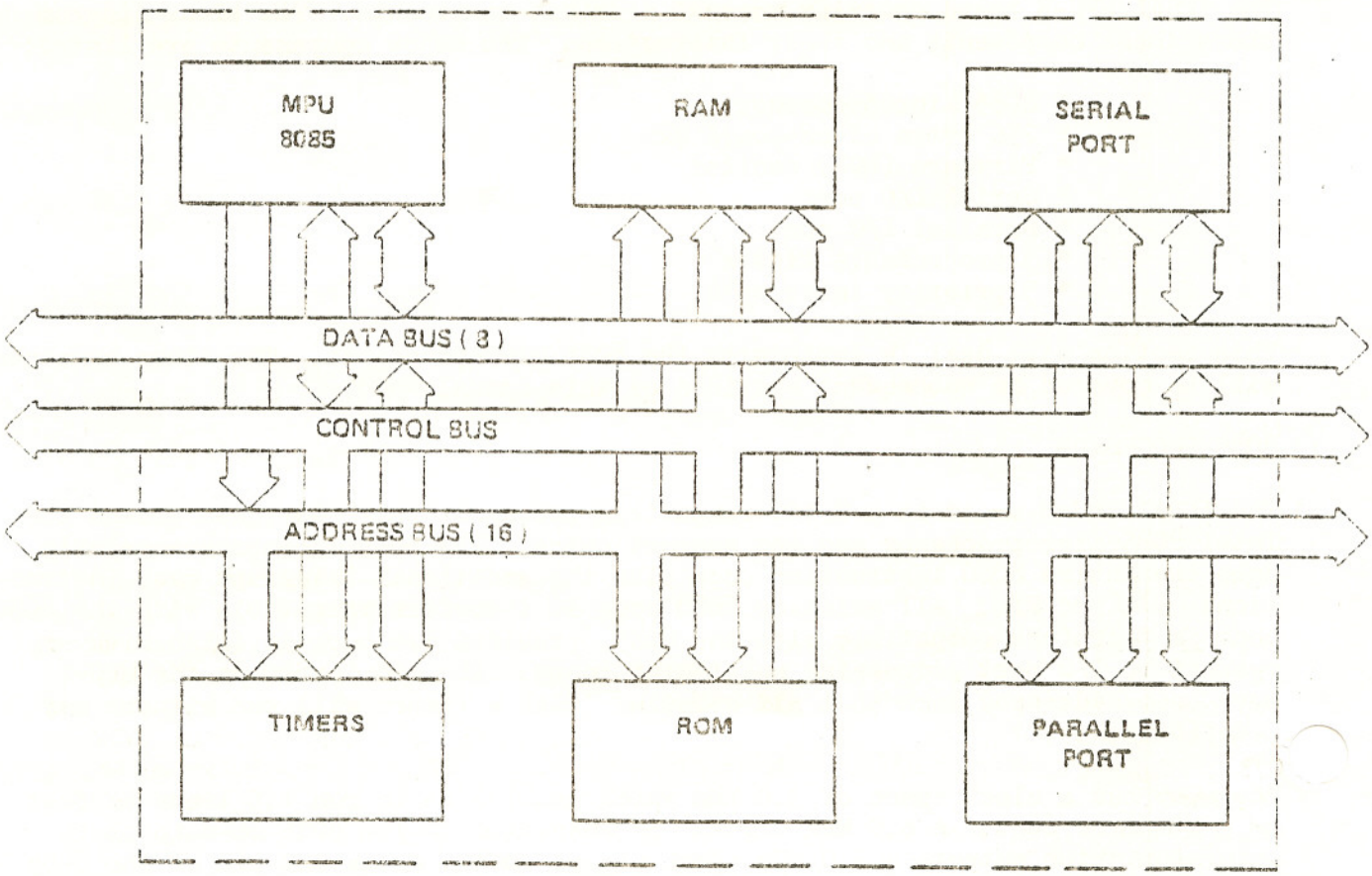
* 8085 Microprocessor
* 256 bytes of on-board RAM
* Firmware (ROM) monitor
* Serial I/O port
* Parallel I/O port
* 3 programable timers
* 5 priority interrupts

This section will deal in depth with the 8085 Microprocessor. The other components will be covered in subsequent sections of this manual.

8085 PROCESSOR

The IMSAI MPU-B board is a S-100 compatible processor board designed around the Intel 8085 microprocessor and its support chips. The 8085 microprocessor chip uses the entire 8080 instruction code plus the additional interrupt mask instructions SIM and RIM. All existing 8080 code is therefore compatible with the 8080 code is therefore compatible with the 8085, provided due care is taken with respect to I/O port addressing and timing loops. The I/O ports on the MPU-B have been addressed such that all existing IMSAI software will run without any modification.

The 8085 has a clock speed of 3.0 MHz which enables it to run 1.5 times as fast as a standard 8080. A 6.0 MHz crystal is connected to the 8085 on-chip clock generator which outputs a 3.0 MHz clock signal on the clock out pin of the 8085 Although the 8085 uses a 3.0 MHz clock, a 2.0 MHz signal is output at pin 49 on the S-100 bus so that other S-100 bus boards may be used with the faster MPU-B. The clock lines, phase 1 and phase 2 run at the higher 3.0 MHz clock rate. Although the 8085 runs 1.5 times as fast as the standard 8080, all bus signals have adequate timing margins due to the 8085's more efficient use of the bus.



POWER REQUIREMENTS

The MPU-B circuitry requires four voltages, +5, -5, +12. The plus and minus 12 volts for RS-232 drivers, pull-up resistors, and the ROM are regulated by TO-220 style, three terminal regulators. Since these TO-220's regulate only a small amount of current, they are heatsinked to the foil on the board. The -5 volts for the ROM is regulated by a TO-220 regulator in series with the -12 volt regulator. The +5 volt regulator is a TC-3 device, mounted on a heatsink. The MPU-B +5 volt current drain is 1.3 amps typical, with a maximum of 1.6 amps.

A 20 millisecond reset time is provided during both power on and manual resets. Also, the 8085 is held in reset any time should the +5 volt line drop below a safe level. The 8085 will not resume running until +5 volts is restored.

MEMORY MAP AND CONTROL PORT LOCATIONS

There are six circuits on the MPU-B board which reside in the memory or I/O space of the processor. The table below lists the circuits and diagram illustrates their location in either the memory or port map.

1. Firmware (ROM)
2. 256 Bytes RAM (on board)
3. 3 Timers
4. Serial I/O port
5. Parallel I/O port
6. MPU-B control port

Some of these circuits can appear in multiple (redundant) locations, and some can be made to appear/disappear under command of the control port.

CONTROL PORT

MPU-B control port is a single I/O mapped port address (F3). It is a write only port and only two of the eight data bits (bits 6 and 7) are used. The control port effects the three memory mapped circuit components shown in diagram (ROM, RAM, TIMERS). The effect of the control port on each of these circuits is as follows:

FIRMWARE (ROM)

The firmware ROM has the ability to reside at more than one location in memory. Its address in memory is controlled by the last two bits of the byte in the control port. At power on and at any reset time the control port bits are set to 0. When bit 6 is 0 the ROM is enabled and mapped at memory address 0000-07FF. Thus the ROM occupies 0000-07FF during the initial power on or reset sequence. When bit 6 is 1 the ROM is disabled at address 0000-07FF and is assigned to system memory. When the firmware ROM is enabled, system memory address 0000-07FF is available for writes only. When it is disabled, 0000-07FF is available for both reads and writes.

When bit 7 of the control port is 0 the firmware ROM is enabled at memory address D800-DFFF. When bit 7 is 1 the ROM is disabled at D800-DFFF and this location is assigned to system memory. When the firmware ROM is enabled, system memory address D800-DFFF is available for writes only. When it is disabled, D800-DFFF is available for both reads and writes.

The firmware ROM may appear simultaneously at 0000-07FF and D800-8FFF, at either location separately, or it may be completely removed from memory.

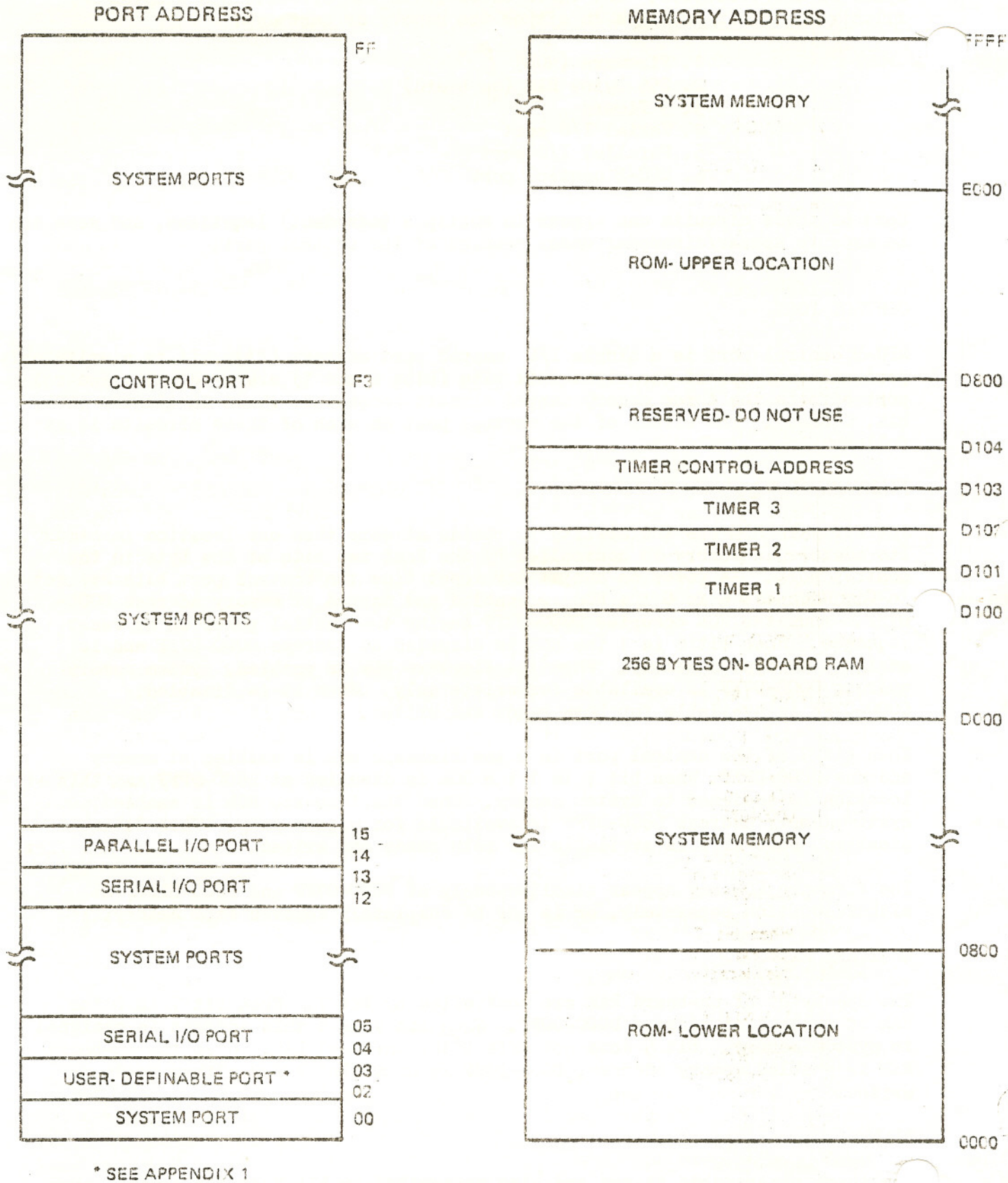
ON-BOARD RAM

The 256 bytes of on-board RAM are controlled by bit 7. When bit 7 is 0 the RAM is enabled at address D000-D0FF. When bit 7 is 1 this address is assigned to system memory. Bit 6 does not effect the on-board RAM. When the on-board RAM is enabled memory address, D000-D0FF is unavailable for either reads or writes.

TIMERS

The three programable timers are also controlled by bit 7 of the control port. When bit 7 is 0 the timers and their control addrss are enabled at location D100-D103. When bit 7 is 0 the timers are disabled and this address is assigned to system memory. When the timers are enabled, the addresses in memory which they occupy are unavailable for either reads or writes.

FIGURE 2


PORT ADDRESS
FF
SYSTEM PORTS
CONTROL PORT
F3
SYSTEM PORTS
15
PARALLEL I/O PORT
14
13
SERIAL I/O PORT
12
SYSTEM PORTS
05
SERIAL I/O PORT
04
03
USER- DEFINABLE PORT *
02
SYSTEM PORT
00
* SEE APPENDIX 1
MEMORY ADDRESS
FFFF
SYSTEM MEMORY
E000
ROM- UPPER LOCATION
D800
RESERVED- DO NOT USE
D104
TIMER CONTROL ADDRESS
D103
TIMER 3
D102
TIMER 2
D101
TIMER 1
D100
256 BYTES ON- BOARD RAM
D000
SYSTEM MEMORY
0800
ROM- LOWER LOCATION
0000

The combination of circuits above which are controlled by bit 7 can not be enabled/disabled separately. They can only be switched in and out as a group. As a result, the entire block of memory space from D000-DFFF is used for the above circuits when bit 7 is 0 and for system memory when bit 7 is 1. The only exception to this is that writes may be made into system memory at address D800-DFFF at all times since this address is occupied by ROM when bit 7 is 0.

The current status of the circuits controlled by the control port may be read by the processor. The status code appears in the status byte from the parallel port 15, bits 6 and 7. The capacity to read this status permits a system to use interrupt routines which can sense the system status, modify it as necessary to service the interrupt, and return it to its original state before returning.

The processor controls the port by writing to it a data byte which has the appropriate code in bits 6 and 7. For example, if the user wanted to disable all of the on-board memory mapped circuits, bits 6 and 7 would both have to 1s. Therefore, the user would write C0 to the control port to accomplish this. When executing a write command to control port, the user must be aware that there in a 3 instruction cycle delay before the commanded change in status takes place. The programmer must be certain that no interrupts occur during these three cycles, as interrupt cycles will be counted. DMA cycles do not affect the 3 cycle delay, however.

ON-BOARD RAM

There are 256 bytes of RAM provided on the MPU-B board. The RAM is located at D000-D0FF, and may be enabled/disabled under software control by using the control port. The upper portion of the on-board RAM area is used for variable storage by the monitor program in the ROM. The rest of the RAM is free for user storage or programs. If the monitor is not to used, not any routines in the ROM called, then the entire 256 bytes may be safely used.

When the on-board RAM is enabled, it has priority over any system memory which shares the same address location. Any time the program enables or disables the RAM, there is a 3 cycle delay before the status change takes place to allow for a jump or call if desired. Information is not lost in either the 256 bytes of RAM or in the system memory when they are enabled or disabled.

The MPU-B board is supplied with a 2K ROM which contains the monitor facilities, power on system initialization, and boot program. The monitor includes loaders for floppy disk, cassette tape and paper tape, as well as extensive machine language entry and debugging features. The monitor will automatically run from either the serial interface or a keyboard and V10.

The firmware ROM has a selectable address. It may appear at memory location 0000-07FF and/or D800-DFFF. The location is under the command of the control port. The operation eration of the ROM is identical in either location, with the following exception. With the ROM at 0000-07FF a routine may access the entire 65K of memory space of the 8085 for complete system initialization. When the ROM is located at D800-DFFF, however, write operations are restricted from D000-D7FF as the 256 byte RAM and the timers are located there.

Under normal operation, the ROM is initially at location 0000-07FF at power on or after a reset. The firmware contains a command which writes an instruction to the control port to disable the ROM at 0000 and enable it at D800-DFFF. The ROM will remain there unless the user relocates it back to 0000 or disables it completely. The monitor commands B,F, and Q will also disable the ROM at D800-DFFF. F and Q will also disable the ROM at 0000-07FF

The IMSAI 2K monitor is stored in the ROM chip supplied with the MPU-B board. The remainder of this section will deal with the monitor's operation and commands.

MONITOR OPERATION

All monitor commands may be executed by simply typing the command with any required parameters and then hitting the carriage return key. Any command can be aborted before hitting the carriage return key by typing CTRL-C. Any time a Hex address parameter is requested from the user, any number of hex digits will be accepted, but only the last 4 will be used. Also, the user is not required to add filler 0's. For example, if the user wishes to input the 16 bit value 002C it may be entered as 2C. Note that this is only true for addresses, data parameters must have 2 characters. Once a monitor command has been initiated, it may be terminated before execution is complete by typing any key on keyboard.

MONITOR COMMAND SUMMARY

A - Adjust and align cassette recorder
B - Boot system
C - Call memory
E - Examine and modify memory
F - Fill memory
G - Generate sync stream
H - Load Intel hex paper tape
I - Perform direct input
J - Jump to memory
K - Switch out MPU-B and jump to address
L - Load cassette file
M - Move memory
N - Relocate disk command string address
O - Perform direct output
P - Protect memory
Q - Switch out MPU-B and jump to VIO monitor
R - Read from diskette
S - Search memory
T - Memory diagnostic
U - Unprotect memory
V - Verify memory
W - Write to diskette
X - Execute from cassette file
Y - Relocate I/O RAM
Z - Select baud rate
:D - Diskette allocation
:I - Input allocation
:O - Output allocation

PARALLEL I/O PORT

The parallel I/O provides a complete 8-bit parallel port with handshaking and latching available in both directions. In most applications the parallel port is used by the monitor for keyboard input. However, the monitor can use the serial port so that the parallel port may be used for any other parallel interfaced device.